

V0.00 Preliminary

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REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Original	Kevin	SW	Dennis	2010/11/3

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1 DESCRIPTION

1.1 Purpose of this Document

This document has been created to provide complete reference specifications for the NT35510. IC design engineers should refer to these specifications when designing ICs, test engineers when testing the compliance of manufactured ICs to guarantee their performance, and application engineers when helping customers to make sure they are using this IC properly.

1.2 General Description

The NT35510 device is a single-chip solution for a-Si TFT LCD that incorporates gate drivers and is capable of 480RGBx864, 480RGBx854, 480RGBx800, 480RGBx720, 480RGBx640 with internal CGRAM. It includes a 9,953,280 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The NT35510 supports MDDI interface, MIPI Interface, 16/18/24 bits RGB interface, 8/16/24-bit system interfaces, serial peripheral interfaces (SPI) and I2C interface. The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The NT35510 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 864-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption.

This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA..

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2 FEATURES

- Single chip WVGA a-Si TFT LCD Controller/driver with Display RAM.
- Display resolution option
 - 480RGB x 864 with 480x24-bitsx 864 GRAM
 - 480RGB x 854 with 480x24-bitsx 854 GRAM
 - 480RGB x 800 with 480x24-bitsx 800 GRAM
 - 480RGB x 720 with 480x24-bitsx 720 GRAM
 - 480RGB x 640 with 480x24-bitsx 640 GRAM
- Display data RAM (frame memory): 480 x 864 x 24-bits = 9,953,280 bits
- Display mode (Color mode)
 - Full color mode: 16.7M-colors
 - Reduce color mode: 262K colors
 - Reduce color mode: 65K colors
 - Idle mode: 8-colors
- Interface
 - 8-/16-/24-bits 80-series MPU interface
 - 16-bit serial peripheral interface
 - I2C interface
 - 16-/18-/24-bits RGB interface (DE mode and SYNC mode with polarity of HS/VS can be set by register)
 - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)
 - Mobile Display Digital Interface (MDDI V1.2, 1 strobe and 1 or 2 data lane pairs)
- Display features
 - Window address functions for specifying a rectangular area on the internal RAM to write data
 - Individual gamma correction setting for RGB dots
 - Deep standby function
- ♦ On chip
 - VGHO/VGLO voltage generator for gate control signal and panel
 - Oscillator for display clock
 - Supports gate control signals to gate driver in the panel
 - On module color characteristics
 - On module checksums checking
 - Four GPO (General Purpose Output) pins for external control

♦ Supply voltage range

- I/O supply voltage range for VDDI to VSSI: 1.65V ~ 3.3V (VDDI) or 1.1 ~ 1.3V (VDDIL)
- Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR: 2.3V ~ 4.8V
- MIPI/MDDI regulator supply voltage range for VDDAM to VSSAM: 2.3V ~ 4.8V

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- Output voltage levels
 - Positive gate driver voltage range for VGH: AVDD+VDDB ~ 2xAVDD AVEE
 - Negative gate driver voltage range for VGLX: AVEE+VCL ~ 2xAVEE-AVDD
 - Step-up 1 output voltage range for AVDD: 4.5 $\sim 6.5 V$
 - Step-up 2 output voltage range for AVEE: -4.5 \sim -6.5V
 - Positive gamma high voltage range for VGMP: 3.0 \sim 6.3V (AVDD-0.3V)
 - Positive gamma low voltage range for VGSP: 0.0, 0.3 \sim 3.7V
 - Negative gamma high voltage range for VGMN: -3.0 ~ -6.3V (AVEE+0.3V)
 - Negative gamma low voltage range for VGSN: 0.0, -0.3 ~ -3.7V
 - Common electrode voltage range for VCOM: 0.0 ~ -3.5V (VCL+0.3V)
 - Panel voltage range for VRGH: 1.0V ~ 6.0V(AVDD-0.3V)

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3 BLOCK DIAGRAM



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4 PIN DESCRIPTION

4.1 Power Supply Pins

Symbol	Name	Description			
VDDB	DC/DC Power	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level			
VDDA	Analog Power	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level			
VDDR	Regulator Power	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level			
VDD_DET	Detection Power	Connect to VDDB/VDDA/VDDR for detection.			
VDDAM	MIPI Power	Power supply for MIPI/MDDI analog regulator system			
VDDI	I/O Power	Power supply for interface system except MIPI/MDDI interface			
DVDD	Digital Voltage	Regulator output for logic system power (1.55V typical) Connect a capacitor for stabilization.			
DIOPWR	Dual I/O Voltage Regulator output for dual I/O voltage system (1.2V/1.8V typical). Connect a capacitor for stabilization.				
MVDDA	MIPI/MDDI Voltage	Regulator output for internal MIPI/MDDI analog system (1.5V typical) Connect a capacitor for stabilization. If not use MIPI/MDDI interface, please open this pin.			
MVDDL	MIPI Voltage	Regulator output for internal MIPI low power system (1.2V typical) Connect a capacitor for stabilization. If not use MIPI interface, please open this pin			
VSSB	DC/DC GND	System ground for DC/DC converter			
VSSA	Analog GND	System ground for analog system			
VSSR	Regulator GND	System ground for regulator system			
VSSAM	MIPI GND	System ground for internal MIPI/MDDI analog system			
VSSI	I/O GND	System ground for interface system except MIPI/MDDI interface			
DVSS	Digital GND	System ground for internal digital system			
AVSS	Source OP GND	System ground for source OP system.			
MTP_PWR	MTP Power	MTP programming power supply pin (7.5 to 8.0V and 7.75V typical) Must be left open or connected to DVSS in normal condition.			



4.2 80-System Interface Pins

Symbol	I/O	Description					
CSX	Ι	hip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. his pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.					
WRX / SCL / I2C_SCL	I	WRX: Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.					
RDX	I	Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface. This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.					
D/CX	Ι	Display data / command selection in 80-series MPU I/F. D/CX = "0" : Command D/CX = "1" : Display data or Parameter This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.					
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For 8080-series MPU I/F: 8-bit interface: D[7:0] are used, D[23:8] should be connected to VSSI 16-bit interface: D[15:0] are used, D[23:16] should be connected to VSSI 24-bit interface: D[23:0] are used These pins are not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI these pins.					

NOTE: "1" = VDDI level, "0" = VSSI level.

4.3 SPI /I2C Interface Pins

NOTE: "1" = VDDI level, "0" = VSSI level.							
4.3 SPI /I2C Interface Pins							
Symbol	1/0	Description					
CSX	11	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.					
WRX/SCL/ I2C_SCL	1	Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.					
SDI / I2C_SDA	SCL: Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCI						
SDO O Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL s SDO O Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL s the host places the SDI line into high-impedance state during the read interval, the SDI a can be tied together. This pin is not used for 80-series MPU, I2C, MIPI or MDDI I/F, please open this pin.							

NOTE: "1" = VDDI level, "0" = VSSI level.



4.4 RGB Interface Pins

Symbol	I/O	Description
PCLK	I	Pixel clock signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
VS	I	Vertical sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
HS	I	Horizontal sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
DE	Ι	Data enable signal in RGB I/F mode 1. This pin is not used for RGB mode 2, 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For RGB I/F: 16-bit/pixel: D[20:16]=R[4:0], D[13:8]=G[5:0] and D[4:0]=B[4:0], connect unused pins to VSSI 18-bit/pixel: D[21:16]=R[5:0], D[13:8]=G[5:0] and D[5:0]=B[5:0], connect unused pins to VSSI 24-bit/pixel: D[23:16]=R[7:0], D[15:8]=G[7:0] and D[7:0]=B[7:0] These pins are not used for MIPI or MDDI I/F, please connect to VSSI these pins.

NOTE: "1" = VDDI level, "0" = VSSI level.

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4.5 MIPI/MDDI Interface Pins

Symbol	I/O	Description						
HSSI_CLK_P HSSI_CLK_N	I	-These pins are N -HSSI_CLK_P/N a that the COG res	These pins are DSI-CLK+/- differential clock signals if MIPI interface is used. These pins are MDDI_STB_P/M differential strobe signals if MDDI interface is used. HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM. These pins are DSI-D0+/- differential data signals if MIPI interface is used. These pins are MDDI_DATA0_P/M differential strobe signals if MDDI interface is used. HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.					
HSSI_D0_P HSSI_D0_N	I/O	-These pins are N -HSSI_D0_P/N ar that the COG res						
HSSI_D1_P HSSI_D1_N	I	-These pins are N -HSSI_D1_P/N ar that the COG res	These pins are DSI-D1+/- differential data signals if MIPI interface is used. These pins are MDDI_DATA1_P/M differential strobe signals if MDDI interface is used. HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.					
ERR	0	When this pin is a	CRC and ECC error output pin for MIPI interface. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found. If not used, please open this pin.					
LANSEL		Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface. LANSEL Data Lane of MIPI/MDDI 0 1 data lane 1 2 data lanes If not used, please connect to VSSI.						
Input pin to select HSSI_D0/D1 data lane sequence a For MIPI interface, both DSWAP and PSWAP function For MDDI interface, only PSWAP function is available					AP function ar s available. Pl	e available. ease connect	DSWAP pin	to VSSI.
I de	Pin Name HSSI_D0_P HSSI_D0_N HSSI_CLK_P HSSI_CLK_N HSSI_D1_P HSSI_D1_ DSWAP=0 DSI-D0+ DSI-D0- DSI-CLK+ DSI-CLK- DSI-D1+ DSI-D1-							
DSWAP PSWAP		Input MIPI	DSI-D0-	DSI-D0+	DSI-CLK-	DSI-CLK+	DSI-D1-	DSI-D1+
MIPI DSWAP=1 Signal DSI-D1+ PSWAP=0 DSI-D1- DSI-CLK+ DSI-CLK- DSI-D0+							DSI-D0-	
	DSWAP=1 PSWAP=1 DSI-D1- DSI-D1+ DSI-CLK- DSI-CLK+ DSI-D0- DSI-D0+							DSI-D0+
		If not used, please connect to VSSI.						



4.6 Interface Logic Pins

Symbol	I/O		Des	cription											
		Signal is active low	It the device and must be a ange for RESX pin is relate												
		Input Voltag	e Level (DSTB_SEL="0")	Min.	Max.	Unit									
		VDDI=1.65~3.3V	Logic High level input vo	tage 0.7xVDDI	VDDI	V									
		VDDI=1.03 0.0V	Logic Low level input vol	tage VSSI	0.3xVDDI	V									
		VDDI=1.1~1.3V	Logic High level input vo	-	1.35	V									
RESX	Ι		Logic Low level input vol	tage VSSI	0.55	V									
		Input Voltage Lev	el(DSTR_SEL=~1~)	DDI=1.65~3.3V	<u> </u>	1.1~1.3V	Unit								
				1in. Max.	Min.	Max.	N								
			· · · · · ·	VDDI VDDI SSI 0.3xVDDI	1.155 VSSI	0.585	V								
		- 0	, ş	.88 1.35V	0.88	1.35V	V								
		<u> </u>		SSI 0.55	VSSL	0.55	V								
		- 3				1	-								
TE			ut pin to synchronize MCU		activated by S	W commar	nd.								
(TE_L)	0		t activated, this pin is output	it low.											
		If not used, please		to france uniting			a d								
TE_R	0		ut pin to synchronize MCU gnal as TE (TE_L) pin.	to manne whiting, a	activated by S	S/W Comman	iū.								
	n Ă	If not used, please open this pin.													
			tion. The connections of I	A[3:0] which not s	hown in table	are invalid.									
		IM[3:0]	Display Data		Command										
		0000 80-serie	es 8-bit MPU I/F, D[7:0]	80-series 8-bit N	MPU I/F, D[7:	0]									
		0001 80-serie	s 16-bit MPU I/F, D[15:0]	80-series 16-bit	MPU I/F, D[1	15:0]									
			s 24-bit MPU I/F, D[23:0]	80-series 24-bit	MPU I/F, D[2	23:0]									
		0011 RGB I/F	, D[23:0]	16-bit SPI (SCL											
			, D[23:0]	16-bit SPI (SCL		trigger), SDI	/SDO								
IM[3:0]			, D[23:0]	I2C I/F, I2C_SD	A										
1010.01		0101 MIPI DS		MIPI DSI,											
		HSSI_D	0_P/N, HSSI_D1_P/N	HSSI_D0_P/N,											
		0110 MDDI,		MDDI, HSSI_D											
			0_P/N, HSSI_D1_P/N	16-bit SPI (SCL			SDO								
		1110 MDDI,	0 P/N, HSSI D1 P/N	MDDI, HSSI_DO 16-bit SPI (SCL	_ / _		/900								
		MDDI,	<u>יט_ו /וא, ווטטו_ר /וא</u>	MDDI, HSSI_D			300								
		1 0111 1	0 P/N, HSSI D1 P/N	12C I/F, 12C SD											
		_	path control in RGB inter												
			y data written to frame me												
RGBBP	I		y data written to line buffer		v pass mode)									
		•	ther interfaces, please cor	· ·	, ,	,									
			••												



		Select the I2C	interface ad	dress fro	m MPU Ifr	ot used, please conr	nect to VS	SI
		I2C SA0			lave Addres			
I2C_SA0	Ι	0			10011 00			
		1			10011 01			
		Input pin to sw		•				
						EDPWM, LEDON, KE	BBC pins.	
		The VSEL dua	al IO function	is valid	when DSTB			
		DSTB_SEL	VDDI	VSEL	DIOPWR	Output	Voltage L	LEDON
		DSTD_SEL	VDDI	VOLL	DIOFWIN	TE		LEDPWM
			1.65~3.3V				1	
		0	or	х	Off	VOH=VDDI		H=VDDI or VDDA
			1.1~1.3V			VOL=VSSI		L=VSSI
				Low	1.2V	VOH=1,2V		H=1.2V
VSEL	I.	1	1.65~3.3V	LOW	1.2 V	VOL=VSSI		L=VSSI
VOLL	'			High	1.8V	VOH=VDDI or DIOI		H=VDDI or VDDA
						VOL=VSSI VOH=1.2V		L=VSSI H=1.2V
			\bigcirc	Low	1.2V	VOH=1.2V VOL=VSSI		H=1.2V L=VSSI
		1	1.1~1.3V			VOH=1.8V		H=1.8V
				High	1.8V	VOL=VSSI		L=VSSI
	~	The input volta	age range for	VSEL	oin:		•	
	1		oltage Level		vlin. Max	. Unit		
	112	Logic High le).88 VDE	N V		
		Logic Low le			SSI 0.55	5 V		
	~	If not used, ple		-			001	
GPO[3:0]	0	General purpo				e swing is VDDI to V	SSI.	
VGSW[3:0]	Ι	Input pin to se						
		Input pin to se	lect the exter			, and the second		
EXB1T		EXB1T 0			VDD Voltage nal DC/DC f			
EADII	I	1			nal DC/DC f			
		If not used, ple						
						1/055		
		Input pin to se		• ·				
NBWSEL	Ι	NBWSEL			55 voltage se			
		0				(Normally White) (Normally Black)		
			• • • •		. , ,	(Normally Diack)		
		Input pin to co		-				
DSTB_SEL	I	DSTB_SEL		WR Reg		VSEL Function	on	
	•	0				Invalid		
		1	D	IOPWR	Un	Valid		

NOTE: "1" = VDDI level, "0" = VSSI level.

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4.7 Driver Output Pins

Symbol	I/O	Description
S1 ~ S1440	0	Pixel electrode driving output.
GOUT1 ~ GOUT32	0	Gate control signals for panel. The swing voltage level is VGHO to VGLO
SDUM0~3	0	Dummy Source, leave it Open if not used
VGHO	0	High voltage level for gate control signals and gate circuit of panel.
VGLO	0	Low voltage level for gate control signals and gate circuit of panel.
LVGL	0	Low voltage level for gate circuit of panel.
VCOM	0	Regulator output for common voltage of panel. Connect a capacitor for stabilization.
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4.8 DC/DC Converter Pins

Symbol	I/O	Description
AVDD	0	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
AVEE	0	Output voltage from step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VCL	0	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	0	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGLX	0	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
VGL	I	Substrate voltage for driver IC. Please connect VGL to VGLX.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	0	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	0	Capacitor connection pins for the step-up circuit which generate AVEE, Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	0	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	0	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	0	Capacitor connection pins for the step-up circuit which generate VGLX. Connect capacitor as requirement.
VRGH	0	Output voltage generated from AVDD. Connect a capacitor for stabilization. When not in use, please open this pin.
VGL_REG	0	Output voltage generated from VGLX. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
EXTP	0	PFM1 control output for DC/DC converter to generate AVDD. Connect to gate of external NMOS device. When not in use, please open this pin.
EXTN	0	PFM2 control output for DC/DC converter to generate AVEE. Connect to gate of external PMOS device. When not in use, please open this pin.
CSP	I	Current sensing input for PFM1 DC/DC converter (generate AVDD). When not in use, please connect to VSSB.
CSN	Ι	Current sensing input for PFM2 DC/DC converter (generate AVEE). When not in use, please connect to VSSB.
VREF_PWR	0	Regulator output for power voltage. Connect a capacitor for stabilization.
VREFCP	0	Reference voltage for internal voltage generating circuit. Connect capacitor for stabilization.

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Symbol	I/O	Description
VGMP	0	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	0	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VGMN	0	Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.
VGSN	0	Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.

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4.9 LABC and CABC Control Pins

Symbol	I/O	Description
LEDON	0	This pin is connect to the external LED driver. It is a LED driver control signal which is used for turning ON/OFF the LED backlight. If not used, please open this pin.
LEDPWM	0	This pin is connect to the external LED driver. It is a PWM type control signal for brightness of the LED backlight. The width of LEDPWM signal is set from 256 values between 0% (Low) and 100% (High) If not used, please open this pin.



4.10 Test Pins

Symbol	I/O	Description
PADA1 PADA2 PADA3 PADA4 PADB1 PADB2 PADB3 PADB4	I/O	 These test pins for chip attachment detection. PADA1 to PADA4 are output pins and PADB1 to PADB4 are input pins. For normal operation: Connect PADA1 and PADB1 together by ITO trace. Connect PADA2 and PADB2 together by ITO trace. Connect PADA3 and PADB3 together by ITO trace. Connect PADA4 and PADB4 together by ITO trace.
CONTACT1A, CONTACT1B, CONTACT2A, CONTACT2B	I/O	- Test pin, for test bonding quality, IC internal will connect CONTACT1A with CONTACT1B, CONTACT2A with CONTACT2B
AVSS_AVDD	I	Test pin, must be connected to AVSS
AVEE_AVSS	I	Test pin, must be connected to AVEE
VCL_VDDB	I	Test pin, must be connected to VCL
VCL_AVSS	Ι	Test pin, must be connected to VCL
VGMN_VGMP	I	Test pin, must be connected to VGMN
VGSN_VGSP	I	Test pin, must be connected to VGSN
KBBC	0	Test pin, not accessible to user. Must be left open
TEST0~7	1/0	Test pin, not accessible to user. Must be left open.
OSC_TEST	I/O	Test pin, not accessible to user, Must left open
VDDI_OPT1~2	0	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSI_OPT1	0	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSIDUM0~106	0	-These pins are dummy with VSSI potential (not have any function inside). -Signal traces can't pass through on glass under these pads.



5 FUNCTIONAL DESCRIPTION

5.1 MPU Interface

NT35510 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in Table 5.1.1

IM3	IM2	IM1	IMO	SRAM	Register
0	0	0	0	80-series 8-bit MPU interface, D[7:0]	80-series 8-bit MPU interface, D[7:0]
0	0	0	1	80-series 16-bit MPU interface, D[15:0]	80-series 16-bit MPU interface, D[15:0]
0	0	1	0	80-series 24-bit MPU interface, D[23:0]	80-series 24-bit MPU interface, D[23:0]
0	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL rising trigger
1	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL falling trigger
0	1	0	0	RGB interface, D[23:0]	I2C interface, I2C_SDA serial data
0	1	0	1	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N
0	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL rising trigger
1	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL falling trigger
0	1	1	1	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N I2C interface, I2C_SDA serial data
Note:	"X" =	Don't	care.	NODISCI	

Table 5.1.1 Interface Type Selection

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5.1.2 80-series MPU Interface

The MCU uses an 11-wires 8-data or 19-wires 16-data or 27-wires 24-data parallel interface.

The chip-select CSX (active low) enables and disables the parallel interface. WRX is the parallel data write, RDX is the parallel data read and D[23:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[23:0] bits are display RAM data or command parameters. When D/C='0', D[23:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM3,IM2, IM1 and IM0.

The interface functions of 80-series parallel interface are given in *Table 5.1.2.*

Table 5.1.2 Parallel interface function (80-Series)

IM3	IM2	IM1	IMO	Interface	D/CX	RDX	WRX	Function
					0	1	Ŷ	Write 16-bit command, D[7:0]
0	0	0	0	8-bit Parallel	1	1	1	Write 16/18/24-bit display data or 16-bit parameter, D[7:0]
0	0	0	0	o-Dit Farallei	1	↑	1	Read 16/18/24-bit display data, D[7:0]
					1	↑	1	Read 16-bit parameter or status, D[7:0]
					0	1	↑	Write 16-bit command, D[7:0]
0	0	0	4	16-bit Parallel	1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[15:0]
0	0	0	1	10-Dit Parallel	1	1	1	Read 16/18/24-bit display data, D[15:0]
					1	↑	3	Read 16-bit parameter or status, D[15:0]
					0	1	↑	Write 16-bit command, D[23:0]
0	0	4		24-bit Parallel		1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[23:0]
0	0	\sim		24-Dit Farallei	1	↑	1	Read 16/18/24-bit display data, D[23:0]
	\mathbf{C}					↑		Read 16-bit parameter or status, D[23:0]
R		٦ ١	AL L		$\left(\right)$	<i>lle</i>	کر	
N	V			MO				
				V				



5.1.2.1 WRITE CYCLE SEQUENCE

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[23:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').



Fig. 5.1.2 80-Series parallel bus protocol, write to register or display RAM

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5.1.2.2 READ CYCLE SEQUENCE

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



Fig. 5.1.4 80-Series parallel bus protocol, read from register or display RAM

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5.1.2.3 8-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

																			,						
Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	0	0	2Ch
oommania	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	0	0	0	0	0	0	00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R 4	R3	R2	R1	R0	G5	G4	G3	65K-Color
000511	х	Х	х	х	х	х	х	х	х	х	х	х	х	Х	х	х	G2	G1	G0	B4	B 3	B2	B1	B 0	05K-C0101
	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R5	R4	R3	R2	R1	R0	Х	Х	
0006h	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	G5	G4	G3	G2	G1	G0	Х	Х	262K-Color
	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	B5	B4	B3	B2	B1	B 0	Х	Х	
	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R 6	R5	R4	R3	R2	R1	R0	
0007h	х	Х	Х	Х	Х	Х	Х	Х	х	х	Х	Х	Х	Х	Х	Х	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
	х	х	х	х	х	х	х	х	х	х	х	х	х	х	х	х	B 7	B6	B 5	B 4	B 3	B2	B1	B 0	0

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NOTES:

- 1. 2 times transfer is used to transmit 1 pixel data with the 16-bit color depth information.
- 2. The most significant bits are Rx4, Gx5 and Bx4.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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NOTES:

- 1. 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
- 2. The most significant bits are Rx5, Gx5 and Bx5.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 16M colors, RGB is 8-8-8-bit pixel data input



NOTES:

- 1. 3 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.
- 2. The most significant bits are Rx7, Gx7 and Bx7.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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5.1.2.4 16-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

=														~~p					· · · ·					0.0.	••
Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	Х	Х	Х	Х	Х	Х	Х	Х	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B 3	B2	B1	B 0	65K-Color
	Х	Х	Х	Х	Х	Х	Х	Х	R 5	R4	R3	R2	R1	R 0	Х	Х	G5	G4	G3	G2	G1	G0	Х	Х	
0006h	Х	Х	Х	Х	Х	Х	Х	Х	B 5	B 4	B3	B2	B1	B0	Х	Х	R 5	R4	R3	R 2	R1	R0	Х	Х	262K-Color
	Х	Х	Х	Х	Х	Х	Х	Х	G5	G4	G3	G2	G1	G0	Х	Х	B5	B 4	B 3	B2	B1	B 0	Х	Х	
	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R 6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	
0007h	х	х	х	х	х	х	х	х	B7	B6	B5	B4	B 3	B2	B1	B 0	R 7	R6	R5	R4	R3	R2	R1	R0	16.7M-Color
	х	х	Х	Х	х	х	Х	Х	G7	G6	G5	G4	G3	G2	G1	G0	B 7	B6	B5	B4	B 3	B2	B1	B 0	

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- 1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.
- 2. The most significant bits are Rx4, Gx5 and Bx4.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
- 2. The most significant bits are Rx5, Gx5 and Bx5.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.
- 2. The most significant bits are Rx7, Gx7 and Bx7.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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5.1.2.5 24-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	X	х	х	X	х	х	х	Х	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	Х	Х	Х	Х	Х	Х	Х	Х	R 4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B 4	B 3	B 2	B1	B0	65K-Color
0006h	Х	Х	Х	Х	Х	Х	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B 4	B 3	B2	B1	B0	262K-Color
0007h								R0	G7	G6	G5	G4	G3	G2	G1	G0	B 7	B6	B5	B 4	B3	B2	B1	B0	16.7M-Color

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- 1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.
- 2. The most significant bits are Rx4, Gx5 and Bx4.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 2. The most significant bits are Rx5, Gx5 and Bx5.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 16M colors, RGB is 8-8-8-bit pixel data input



- 1. In one transfer (D23 to D0), 1 pixel data transmitted with the 24-bit color depth information.
- 2. The most significant bits are Rx7, Gx7 and Bx7.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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5.1.2.6 8-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

	Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	ommand	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	1	0	2Eh
Ŭ	onnana	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	0	0	0	0	0	0	00h
		D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	Read	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R6	R5	R 4	R3	R2	R1	R0	
	Data	х	Х	Х	Х	х	х	х	х	х	х	Х	Х	х	х	х	Х	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
		х	Х	х	Х	Х	Х	Х	х	Х	Х	Х	Х	х	х	х	Х	B 7	B6	B5	B4	B 3	B2	B1	B0	



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5.1.2.7 16-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Read	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Data	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
Data	х	х	Х	х	х	х	х	Х	B 7	B6	B5	B4	B 3	B2	B1	B 0	х	Х	Х	х	Х	х	Х	х	10.7 10-000



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5.1.2.8 24-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	х	х	х	X	х	х	х	х	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Read	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Data								R0	G7	G6	G5	G4	G3	G2	G1	G0	B 7	B6	B5	B 4	B 3	B2	B1	B0	16.7M-Color



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5.1.3 Serial Interface

The selection of this interface is done by IM3, IM2, IM1 and IM0.

The serial interface can select IM3 = 0 or 1 to decide the trigger edge of serial clock (SCL) is rising edge or falling edge. The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

5.1.3.1 WRITE MODE

The write mode of the interface means the micro controller writes commands and data to the NT35510. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low (see *Fig. 5.1.5*). SDI/SDO are sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

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Fig. 5.1.5 Serial bus protocol for register write mode

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5.1.3.2 READ MODE

The read mode of the interface means that the micro controller reads register value from the NT35510. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send (see *Fig. 5.1.6*). The NT35510 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (16 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

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Fig. 5.1.6 Serial bus protocol for register read mode

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5.1.3.3 SERIAL INTERFACE FOR DATA RAM WRITE

The serial interface is used with RGB interface (IM[2:0]="011") or MDDI interface (IM[2:0]="110"). In RGB+SPI interface, the data RAM write function for SPI is valid when bit ICM="1" (command B300h of page 0). In MDDI+SPI interface, the data RAM write function for SPI is valid when MDDI is not writing data to RAM. Different display data formats are available for three color depths supported by the LCM listed below:

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- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3A00h is 0x0005)

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- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3A00h is 0x0006) First Transmit s P Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) տուրուներուներ านน SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z Command / Address and / Address Transmission d / Address High Byte Trans 8-bit 8-bit Second Transmit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) տուրուներուներուներ ENIL SDI (Host to Driver IC) R/W D/CX H/L 0 SDO (Driver IC to Host) High-Z High-Z High-Z R/W = 0 for Writing 0 D/CX = 0 for Comma H/L = 0 for Comman and / Address Transmission nird Transmit (Red) PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z W = 0 for Writing HAM Data CX = 1 for RAM Data Transmission L = 0 for RAM Data Low Byte Transm Fourth Transmit (Green) PS smission Byte Trans CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z ata Transmission ta Low Byte Trans 8-bit ifth Transmit (Blue) s PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) JIII (Rising Edge, IM3 = 0, SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบา SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z R/W = 0 for Writing RAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transmis 8-bit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบบ $1 \Box \Box \Box$ SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z H/W = 0 for Writing HAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transr

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First Transmit PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) տուրուներուներ านน SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z Command / Address and / Address Transmission d / Address High Byte Trans 8-bit 8-bit Second Transmit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) տուրուներուներուներ ENIL SDI (Host to Driver IC) R/W D/CX H/L 0 SDO (Driver IC to Host) High-Z High-Z High-Z R/W = 0 for Writing 0 D/CX = 0 for Comma H/L = 0 for Comman and / Address Transmission nd / Address Low Byte Trans nird Transmit (Red) PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z W = 0 for Writing RAM Data CX = 1 for RAM Data Transmission - = 0 for RAM Data Low Byte Transm Fourth Transmit (Green) PS mission Byte Tran CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) TTTT. SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z ata Transmission ta Low Byte Trans 8-bit ifth Transmit (Blue) s PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) JIII (Rising Edge, IM3 = 0, SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบา SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z R/W = 0 for Writing RAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transmi 8-bit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบบ $1 \Box \Box \Box$ SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z H/W = 0 for Writing HAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transr

- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3A00h is 0x0007)

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5.1.3.4 SERIAL INTERFACE FOR DATA RAM READ

The read data RGB is 8-8-8-bit output as below.



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5.2 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I2C-Bus Protocol:

Before any data is transmitted on the I2C-bus, the device, which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.



(b) Definitions:

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



Fig. 5.2.2 System Configuration



5.2.1 Slave Address of I2C

NT35510 supports two slave addresses, 1001100, 1001101 after the START procedure via I2C bus for MCU usage .There are 1 hard pin, I2C_SA0 to determine the difference slave address. The slave address selection is described as the following table. The I2C interface address is selected from the external MPU.

I2C_SA0	Slave Address	Notes
0	1001100	0000xxx and 1111xxx: Reversed
1	1001101	

Table 5.2.1 Selection Table of Slave Address

5.2.2 Register Write Sequence of I2C Interface

NT35510 supports register write sequence via I2C-bus transfer. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in Fig.5.2.2.

- (2) After the START condition (S), a slave address is sent. R/W bit is setting to "zero" for WRITE.
- (3) The slave issues an ACK to master.
- (4) 16 bits register high byte address transfer first. Then transfer the register low byte address.
- (5) 16 bits register high byte data of parameter transfer first. Then transfer the register low byte data parameter.
- (6) A data transfer is always terminated by a STOP condition.



5.2.3 RAM Data Write Sequence of I2C Interface

NT35510 supports sequential RAM data writing via I2C-Bus. NT35510 will increase the RAM address automatic by window address when the Host MCU write the RAM data via this way. The transfer protocol of window address setting can refer to the 5.2.3 Register Write Sequence. Different display data formats are available for three color depths supported by the LCM.

The sequential RAM writing timing is shown in below.





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5.2.4 Register Read Sequence of I2C Interface

NT35510 supports register read sequence via I2C-bus transfer. Register data reading transfers follow the format and is shown in Fig.5.2.4.



Register Write Sequence. Then the master MCU need to send the BAM data read register "2E00h" to NT35510. And finally, the MCU can send the following RAM data reading timing to feedback single RAM data value by one complete I2C packet.

The RAM data reading timing is shown in below.





W: Write Bit, where W="0" R: Read Bit, where R="1" ACK: Acknowledge Bit, where ACK="0" NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address

ADD[15:0]: Register Address, where ADD[15:0]="0x2E00" R1[4:0], R2[4:0], ..., Rn[4:0]: The red color data of each pixel G1[5:0], G2[5:0], ..., Gn[5:0]: The green color data of each pixel B1[4:0], B2[4:0], ..., Bn[4:0]: The blue color data of each pixel

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W: Write Bit, where W="0" R: Read Bit, where R="1" ACK: Acknowledge Bit, where ACK="0" NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address

ADD[15:0]: Register Address, where ADD[15:0]="0x2E00" R1[5:0], R2[5:0], ..., Rn[5:0]: The red color data of each pixel G1[5:0], G2[5:0], ..., Gn[5:0]: The green color data of each pixel B1[5:0], B2[5:0], ..., Bn[5:0]: The blue color data of each pixel

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NACK: Non-acknowledge Bit, where NACK="1"

G1[7:0], G2[7:0], ..., Gn[7:0]: The green color data of each pixel B1[7:0], B2[7:0], ..., Bn[7:0]: The blue color data of each pixel

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5.3 Interface Pause

By using parallel interface, it is possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the CSX (Chip Select Line) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then NT35510 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the CSX (Chip Select Line) is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the CSX (Chip Select Line) is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

Parallel Interface Pause



Serial Interface Pause

16-bit SPI interface does not support "Pause Mode"

MIPI Interface Pause

Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.

1) Same receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => ...

2) Different receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => ...

The means that "=>" symbol means a pause on DSI.

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5.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example (See *Fig. 5.4.1*)

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example (See *Fig. 5.4.2*)



Fig. 5.4.2 Serial bus protocol, write mode – interrupted by CSX



Display data transfer break is illustrated for reference purposes below. Without break



With break (See and check also exceptions*)



*) See also an exception on section "6.1 User Command Set" and Note 2.

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode

The NT35510 stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.

The break condition can be done any time when the MCU or the driver IC is controlling DSI data lanes e.g. the driver IC is sending data to the MCU.

Except MIPI interface, the data transfer break mechanism illustrated for reference purposes below.





5.5 Display Module Data Transfer Modes

The NT35510 has 3 kinds of color mode for transferring data to the frame Memory. There are 16-bit color per pixel, 18-bit color per pixel and 24-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

Start				_	Stop									
Start Frame Memory Write	Image Data Frame 1	Image Data Frame 2	Image Data Frame 3		Any Command									
	Fig. 5.5.1 Data Transfer Method 1													

Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



1) The Frame Memory can contain odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

2) "Memory Write Continue (3Ch)" or "Memory Read Continue (3Eh)" commands are not stopping writing or reading to/from the frame memory. These commands can be used if there is wanted to continue the writing or reading to/from the frame memory when "Any Command" has stopped the memory writing or reading.

3) "Any Command" can be as same as "Start Frame Memory Write".





5.6 RGB Interface

5.6.1 General Description

For direct interface with both graphic controller and MPU, NT35510 offer RGB interface mode to display video signal. The parallel RGB interface includes: VS, HS, DE, PCLK, D[23:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[23:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative ("0", low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative ("0", low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a positive ("1", high) active and its state is read to the display module by a rising edge of the PCLK signal. D[23:0] (24-bit: R7-R0, G7-G0 and B7-B0;18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE= "1" and there is a rising edge of PCLK). D[23:0] can be "0" (low) or "1" (high). These lines are read by a rising edge of the PCLK signal.



Note: PCLK is an unsynchronized signal (It can be stopped)

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5.6.2 RGB Interface Timing Chart

The image information must be correct on the display, when the timings are in range on the interface.

However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.





5.6.3 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	D23-D0	VS	HS	Register VFP[7:0], VBP[7:0] HFP[7:0], HBP[7:0]
RGB Mode 1 (SYNC + DE)	Used	Used	Used	Used	Used	Not used
RGB Mode 2 (SYNC only)	Used	Not used	Used	Used	Used	Used

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D23 to D0), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to NT35510 DDI.

In RGB Mode 2, back porch of Vsync VBP is defined by VBP[7:0] of RGBCTR command. And back porch of Hsync HBP is defined by HBP[7:0] of RGRCTR command. Front porch of Vsync VFP is defined by VFP[7:0] of RGBCTR command. And front porch of Hsync HFP is defined by HFP[7:0] of RGBCTR command.

Note: VBP[7:0]=Vsync+VBP and HBP[7:0]=Hsync+HBP.

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Fig. 5.6.2 Video signal data writing method in RGB Mode 1 Interface

Notes:

1. Constraint:

V-Back Porch (Vsync+VBP) ≥ 5 HS lines, V-Front-Borch (VFP) ≥ 2 HS lines Vsync+VBP+VFP (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch) H-Back Porch (Hsync+HBP) ≥ 5 PCLK clocks, H-Front-Porch (HFP) ≥ 2 PCLK clocks 2. $t_{VHS} \ge 400$ ns

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Fig. 5.6.3 Video signal data writing method in RGB Mode 2 Interface

Notes:

1. Constraint:

V-Back Porch (VBP[7:0]) \geq 5 HS lines, V-Front Porch (VFP[7:0]) \geq 2 HS lines VBP[7:0]+VFP[7:0] (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch) H-Back Porch (HBP[7:0]) \geq 5 PCLK clocks, H-Back Porch (HFP[7:0]) \geq 2 PCLK clocks 2. $t_{VHS} \geq$ 400ns

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Fig. 5.6.5 RGB with SPI Timing Sequence (Exit Internal Clock Mode, ICM="0")

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5.6.4 RGB Interface Bus Width Set

All 3-kinds of bus width can be available during RGB interface mode (selected by the COLMOD command (3A00h): VIPF[3:0]).

3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
50h	х	х	х	R 4	R3	R 2	R1	R0	х	х	G5	G4	G3	G2	G1	G0	х	х	х	B 4	B 3	B 2	B1	B 0	16-bit data
60h	x	х	R5	R 4	R3	R2	R1	R0	х	х	G5	G4	G3	G2	G1	G0	х	х	B 5	B 4	B 3	B2	B1	B0	18-bit data
70h	R 7	R6	R5	R 4	R3	R 2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B 7	B6	B 5	B 4	B 3	B 2	B1	B 0	24-bit data

NOTES:

1. "x": Unused RGB data bus connected with VSSI.

2. R0 is the LSB for the red component; G0 is the LSB for the green component, etc.

3. For 16-bit pixels, R primary color MSB is R4, G primary color MSB is G5 and B primary color MSB is B4.

4. For 18-bit pixels, R primary color MSB is R5, G primary color MSB is G5 and B primary color MSB is B5

5. For 24-bit pixels, R primary color MSB is R7, G primary color MSB is G7 and B primary color MSB is B7

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Write data for 16-bit RGB interface bus width set is shown below.

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Write data for 18-bit RGB interface bus width set is shown below.

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VS	"1"				
HS	"1"				
DE	"1"				
PCLK		1			
D23		R1, Bit 7	R2, Bit 7	R3, Bit 7	Rn, Bit 7
D22		R1, Bit 6	R2, Bit 6	R3, Bit 6	Rn, Bit 6
D21		R1, Bit 5	R2, Bit 5	R3, Bit 5	Rn, Bit 5
D20		R1, Bit 4	R2, Bit 4	R3, Bit 4	Rn, Bit 4
D19		R1, Bit 3	R2, Bit 3	R3, Bit 3	Rn, Bit 3
D18		R1, Bit 2	R2, Bit 2	R3, Bit 2	Rn, Bit 2
D17		R1, Bit 1	R2, Bit 1	R3, Bit 1	Rn, Bit 1
D16		R1, Bit 0	R2, Bit 0	R3, Bit 0	Rn, Bit 0
D15		G1, Bit 7	G2, Bit 7	G3, Bit 7	Gn, Bit 7
D14		G1, Bit 6	G2, Bit 6	G3, Bit 6	Gn, Bit 6
D13		G1, Bit 5	G2, Bit 5	G3, Bit 5	Gn, Bit 5
D12		G1, Bit 4	G2, Bit 4	G3, Bit 4	Gn, Bit 4
D11	$- \mathcal{H}$	G1, Bit 3	G2, Bit 3	G3, Bit 3	Gn, bit 3
D10	<u>> {{</u>	G1, Bit 2	G2, Bit 2	G3, Bit 2	Gn, Bit 2
09	_ Л`	G1, Bit 1	G2, Bit 1	G3, Bit 1	Gn, Bit 1
D8	2	G1, Bit 0	G2, Bit 0	G3, Bit 0	Gn, Bit 0
D7		B1, Bit 7	B2, Bit 7	B3, Bit 7	Bn, Bit 7
D6	\bigcirc	B1, Bit 6	B2, Bit 6	B3, Bit 6	Bn, Bit 6
	C	B1, Bit 5	B2, Bit 5	B3, Bit 5	Bn, Bit 5
D4	n	B1, Bit 4	B2, Bit 4	B3, Bit 4	Bn, Bit 4
	h_{r}	B1, Bit 3	B2, Bit 3	B3, Bit 3	Bn, Bit 3
		B1, Bit 2	B2, Bit 2	B3, Bit 2	Bn, Bit 2
D1		B1, Bit 1	B2, Bit 1	B3, Bit 1	Bn, Bit 1
DO		B1, Bit 0	B2, Bit 0	B3, Bit 0	Bn, Bit 0
2		Pixel 1	Pixel 2	Pixel 3	 Pixel n
		Ţ			

Write data for 24-bit RGB interface bus width set is shown below.

R1[7] R1[6] R1[5] R1[4] R1[3] R1[2] R1[1] R1[0] G1[7] G1[6] G1[5] G1[4] G1[3] G1[2] G1[1] G1[0] B1[7] B1[6] B1[5] B1[4] B1[3] B1[2] B1[1] B1[0]



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5.7 Frame Memory

5.7.1 Configuration

The NT35510 has an integrated 480 x 864 x 24-bit graphic type static RAM. This 9,953,280-bit memory allows to store on-chip a 480 x RGB x 864, 480 x RGB x 854, 480 x RGB x 800, 480 x RGB x 720 and 480 x RGB x 640 image with an 24-bit resolution (16.7M-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.





5.7.2 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 1-1-1-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The address pointers address the locations of RAM.

When CGM[7:0]="70h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=863 (35Fh).

When CGM[7:0]="6Bh", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=853 (355h).

When CGM[7:0]="50h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=799 (31Fh).

When CGM[7:0]="28h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=719 (2CFh).

When CGM[7:0]="00h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=639 (27Fh).

Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example, the whole display contents will be written when CGM[7:0]="50h", if the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=479 (1DFh), YE=799 (31Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR" (see section 6 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 5.2.2 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

Condition **Column Counter Row Counter** Return to Return to When RAMWR/RAMRD command is accepted "Start Row (YS)" "Start Column (XS)" Twice Increment by 1 Complete Pixel Pair Read / Write action No change (First Pixel n then Pixel n+1) Return to The Column counter value is larger than "End Column (XE)" Increment by 1 "Start Column (XS)" The Column counter value is larger than "End Column (XE)" Return to Return to and the Row counter value is larger than "End Row (YE)" "Start Column (XS)" "Start Row (YS)" NOTE:

For each image condition, the controls for the column and row counters apply as below:

Data is always written to the Frame Memory in the order, regardless of the Memory Write Direction set by command MADCTL (36h) bit MY, MX and MV. The write order for each pixel unit is (R, G, B) transferred from (D2, D1, D0) = (R, G, B). One pixel unit represents 1 column and 1 page counter value on the Frame Memory



5.7.3 Interface to Memory Write Direction

The resultant image for each orientation setting is illustrated below.



NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

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5.7.4 Frame Memory to Display Address Mapping

The frame memory to display address mapping for 480RGB x 864 resolution (RSMX=RSMY="0") is shown below figure. The maximum address of RA/SA/CA and used source outputs are decided by bit CGM[2:0] (see command 2Ah CASET, 2Bh PASET and section 7.2).



RA = Row Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

PTD = Source output voltage selection for 1-bit data "0" and "1", parameter of PWCTR5 command

* RA and CA is exchange when MV = "1"

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5.8 Tearing Effect Information

5.8.1 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.8.1.1 TEARING EFFECT LINE MODES

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh = The LCD display is not updated from the Frame Memory

tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.



thdh = The LCD display is not updated from the Frame Memory thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 3, this mode turn on the Tearing Effect Output signal when vertical scanning reaches line N.



N = The N-th scanning line which set by register N[15:0] of command STESL (44h)

The TE mode selection is described as below table

DOPCTR (B100h)	TEOFF (34h) TEON (35h)	STESL (44h)	TE Output
DSITE	М	N[15:0]	
0	Х	Х	TE off (output low)
1	34h	Х	TE off (output low)
1	35h with M=0	N[15:0]=0	TE high in V-porch region (Mode 1)
1	35h with M=0	N[15:0]≠0	TE high at N-th line (Mode 3)
1	35h with M=1	Х	TE high in all V-porch and H-porch region (Mode 2)

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5.8.1.2 TEARING EFFECT LINE TIMING

The Tearing Effect signal is described below:



Table 5.8.1 AC characteristics of Tearing Effect Signal

Symbol	Parameter min max unit Descriptio	'n
tvdl	Vertical Timing Low Duration TBD - ms	
tvdh	Vertical Timing High Duration 1000	
thdl	Horizontal Timing Low Duration TBD	
thdh	Horizontal Timing High Duration TBD 500 µs	
Notoo		

Notes: 1. The timings in above table apply when MADCTL ML=0 and ML=1.

2. The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns when the maximum load is TBD Ω .

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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5.8.1.3 EXAMPLE 1: MPU WRITE IS FASTER THAN PANEL READ.



Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



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5.8.1.4 EXAMPLE 2: MPU WRITE IS SLOWER THAN PANEL READ.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



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5.9 Checksum

The display module consists of two 8-bit checksum registers, which are used checksum calculations for "User Command Set" area registers (includes the frame memory), on the display module.

One of the checksum registers is "First Checksum" (FCS) and another is "Continue Checksum" (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on "User Command Set" area registers. This means that read commands are not used as a calculation starting trigger in this case.

The checksum calculation is always interrupted, when there is a new write access on Nokia area registers. The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on "User Command Set" area registers and the new checksum value is calculated in the first time again.

The maximum time, when the FCS is readable, is 150ms after there is the last write access on "User Command Set" area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last Nokia area register has been calculated to the checksum.

The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on "User Command Set" area registers.

There is always updated a checksum comparison bit (See section: "Read Display Self-Diagnostic Result (0Fh)" and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

User can read FCS, CCS and Comparison bit D0 values. See section: "Read First Checksum (AAh)", "Read Continue Checksum (AFh)" and "Read Display Self-Diagnostic Result (0Fh)".

There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in "Sleep Out" mode and it is stopped in "Sleep In" mode.



					,	
Step Note1	Time Note2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on "User Command Set" area registers => FCS an CCS registers are initialized
2	0 150ms	Continue sum of "User Command Set" area registers	Counting	-	-	The first register counting is running
3	150ms	Stores sum of registers on FCS register	Set to 00h after value is moved to FCS register	Stores sum of "User Command Set" area registers on FCS register		The result of the first register counting is stored on FCS register. The result of the FCS is available to the MPU
4	150ms 300ms	Continue sum of "User Command Set" area registers	Counting			The second register counting is running
5	300ms	 Stores sum of registers on CCS register Compares stored FCS and CCS value 	Set to 00h after value is moved to CCS register		Stores sum of "User Command Set" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
6	300ms 450ms	Continue sum of "User Command Set" area registers	Counting	SU		The third register counting is running
7	450ms	 Stores sum of registers on CCS register Compares stored FCS and CCS value 	Set to 00h after value is moved to CCS register		Stores sum of "User Command Set" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
8	450 600ms	Continue sum of "User Command Set" area registers	Counting	-	-	The fourth register counting is running
9	600ms	 Stores sum of registers on CCS register Compares stored FCS and CCS value 	Set to 00h after value is moved to CCS register	-	Stores sum of "User Command Set" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
10	etc	-	-	-	-	Same sequence continue e.g. step 4 and 5

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5.10 Power On/Off Sequence

VDDI and VDD (VDDA) can be applied in any order.

VDD (VDDA) and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD (VDDA) and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD (VDDA) can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. *Notes:*

- 1. There will be no damage to the display module if the power sequences are not met.
- 2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
- 3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
- 4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.10.1 and 5.10.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
- 5. There is not a limit for Rise/Fall time on VDDI and VDD (VDDA).
- 6. The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VDD (VDDA) are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.



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5.10.1 Case 1 – RESX line is held High or Unstable by Host at Power On

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD (VDDA) and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.





5.10.2 Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD (VDDA) and VDDI have been applied.



5.10.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.



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5.11 Power Level Modes

5.11.1 Definition

7 level modes are defined they are in order of maximum power consumption to minimum power consumption:

- 1. Normal Mode On (full display), Idle Mode Off, Sleep Out. In this mode, the display is able to show maximum 16.7M colors.
- Partial Mode On, Idle Mode Off, Sleep Out In this mode, part of the display is used with maximum 16.7M colors.
- 3. Normal Mode On (full display), Idle Mode On, Sleep Out. In this mode, the full display is used but with 8 colors.
- 4. Partial Mode On, Idle Mode On, Sleep Out In this mode, part of the display is used but with 8 colors.
- 5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.

6. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory is random.

7. Power Off Mode

In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

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5.11.2 Power Level Mode Flow Chart



NOTES:

There is not any abnormal visual effect when there is changing from one power mode to another power mode.
 There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode



The following table represents the SRAM and Registers its mode state. Control Mode SRAM Register Enter Exit Sleep in mode 1 (RAMKP = 1) Keep Keep Command Sleep in mode 2 (RAMKP = 0) Command Loss Keep Command Deep-standby mode Loss Reset pin Loss Keep Reset=L Reset (H/W) Loss (Default Value) The condition for irregular power off mode is shown below. VDDI VDD RESX **Power Off Mode** I/O Mode 1 ON OFF High or Low Low Mode 2 OFF ON High or Low Low Note: VDD means VDDA, VDDR, VDDB and VDDAM Power Off Condition VDD ON VDDOFF VDD ON VDDI ON VDDI OFF VDDION If VDD turned off If VDDI turned off Power-OFF Mode1 Power-OFF Mode2 Sleep-In Mode If VDDI turned on If VDD turned on

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5.12 Reset function

5.12.1 Register Default Value

Table 5.12.1 Default Values for User Command Set

		After	After	After		
	Item	Power On	Hardware Reset	Software Reset		
RDNUMPE (05	n)	00h	00h	00h		
RDDPM (0Ah)		08h	08h	08h		
RDDMADCTR ((0Bh)	00h	00h	00h		
RDDCOLMOD	(0Ch)	07h	07h	07h		
RDDIM (0Dh)		00h	00h	00h		
RDDSM (0Eh)		00h	00h	00h		
RDDSDR (0Fh)		00h	00h	00h		
Sleep In/Out (10	0h/11h)	In	In	In		
Partial/Normal	Display (12h/13h)	Normal 🦯 👖	Normal	Normal		
Display Inversio	n On/Off (21h/20h)	Off	Off	Off		
All Pixel On/Off	(23h/22h)	Off	Off	Off		
Gamma setting	(26h)	01h (GC0)	01h (GC0)	01h (GC0)		
Display On/Off	(29h/28h)	Off	Off	Off		
Column: Start A	ddress (XS, 2Ah)	0000h	0000h	0000h		
	CGM[7:0]="70h" (480x864)	01DFh (479d)	01DFh (479d)	01DFh (479d)		
Column:	CGM[7:0]="6Bh" (480x854)	01DFh (479d)	01DFh (479d)	01DFh (479d)		
End Address	CGM[7:0]="50h" (480x800)	01DFh (479d)	01DFh (479d)	01DFh (479d)		
(XE, 2Ah)	CGM[7:0]="28h" (480x720)	01DFh (479d)	01DFh (479d)	01DFh (479d)		
	CGM[7:0]="00h" (480x640)	01DFh (479d)	01DFh (479d)	01DFh (479d)		
Row: Start Addr		0000h	0000h	0000h		
V	CGM[7:0]="70h" (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)		
Row:	CGM[7:0]="6Bh" (480x854)	0355h (853d)	0355h (853d)	0355h (853d)		
End Address	CGM[7:0]="50h" (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)		
(YE, 2Bh)	CGM[7:0]="28h" (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)		
	CGM[7:0]="00h" (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)		
Frame memory	(2Ch, 2Eh, 3Ch, 3Eh)	Random	Random	Random		
Partial: Start Ad	dress (PSL, 30h)	0000h	0000h	0000h		
	CGM[7:0]="70h" (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)		
Partial:	CGM[7:0]="6Bh" (480x854)	0355h (853d)	0355h (853d)	0355h (853d)		
End Address	CGM[7:0]="50h" (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)		
(PEL, 30h)	CGM[7:0]="28h" (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)		
	CGM[7:0]="00h" (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)		
Tearing: On/Off	(35h/34h)	Off	Off	Off		



	ne 5.12.1 Delault Va	alues for User Commar				
ltem		After	After	After		
		Power On	Hardware Reset	Software Reset		
Memory Data Access Contr (MY/MX/MV/ML/RGB/MH/F	· · ·	00h	00h	00h		
Idle Mode On/Off (38h/39h)		Off	Off	Off		
Interface Pixel Color Forma	t (3Ah)	77h	77h	77h		
Set Tearing Effect Scan Lin	e (44h)	0000h	0000h	0000h		
Get Scan Line (45h)		N/A	N/A	N/A		
DSTB mode (4Fh)		00h	00h	00h		
Profile Value for Display (50)h)	All values are FFh	All values are FFh	All values are FFh		
Display Brightness (51h, 52	h)	00h	00h 15	00h		
CTRL Display (53h, 54h)		00h	00h	00h		
CABC Control (55h, 56h)		00h	OOh	00h		
Write Hysteresis (57h)		All values are FFh	All values are FFh	All values are FFh		
Write Gamma Setting (58h)		All values are 11h	All values are 11h	All values are 11h		
RDFSVM (5Ah)		00h	00h	// 00h		
RDFSVL (5Bh)		00h	00h	00h		
RDMFFSVM (5Ch)		00h	00h	00h		
RDMFFSVL (5Dh)		00h	00h	00h		
RDLSCCM (65h, 66h)		80h	80h	80h		
RDLSCCL (65h, 67h)		OOh V	00h	00h		
Black/White Color	After MTP	MTP Value	MTP Value	MTP Value		
Characteristics (70h~74h)	Before MTP	00h	00h	00h		
Red/Green Color	After MTP	MTP Value	MTP Value	MTP Value		
Characteristics (75h~79h)	Before MTP	00h	00h	00h		
Blue/AColor Color	After MTP	MTP Value	MTP Value	MTP Value		
Characteristics (7Ah~7Eh)	Before MTP	00h	00h	00h		
DDB Start/Continue (A1h)	After MTP	MTP Value	MTP Value	MTP Value		
	Before MTP	00h	00h	00h		
DDB Continue (A8h)	After MTP	MTP Value	MTP Value	MTP Value		
	Before MTP	00h	00h	00h		
First/Continue Checksum (A	Ah, AFh)	00h	00h	00h		
ID1 (DAh)	After MTP	MTP Value	MTP Value	MTP Value		
ID2 (DBh)		ID1 = "00h"	ID1 = "00h"	ID1 = "00h"		
ID3 (DCh)	Before MTP	ID2 = "80h"	ID2 = "80h"	ID2 = "80h"		
		ID3 = "00h"	ID3 = "00h"	ID3 = "00h"		

Table 5.12.1 Default Values for User Command Set (Continuous)



5.12.2 Output or Bi-directional (I/O) Pins

Output or	Bi-directional pins	After Power On	After Hardware Reset	After Software Reset		
	I_DATA0_P, iI_DATA0_N	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)		
	TE	VSSI	VSSI	VSSI		
SDO	Using SPI	VDDI	VDDI	VDDI		
300	Not using SPI	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)		
Source	e Driver Output	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)		
GOU	T1~GOUT32	AVSS	AVSS	AVSS 🚬		

NOTE: There will be no output from TE, SDO, D23-D0, HSSI_DATA0_P/N and HSSI_DATA1_P/N during Power PATT On/Off sequence, H/W Reset and S/W Reset

5.12.3 Input Pins

	Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
	RESX	See Section 5.10	Input Valid	Input Valid	Input Valid	See Section 5.10
	CSX	Input Invalid	Input Valid	💙 Input Valid 🚺	Input Valid	Input Invalid
	D/CX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	WRX (SCL / I2C_SDA)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	RDX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	D23 to D0	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	SDI (I2C_SCL)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HS	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
\mathbb{N}	vs	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	PCLK	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	DE 🔰	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HSSI_CLK_P, HSSI_CLK_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HSSI_DATA0_P, HSSI_DATA0_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HSSI_DATA1_P, HSSI_DATA1_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid

5.13 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

5.13.1 Register loading Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM values, 2nd step: Loads EEPROM value to register). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of these commands is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1) and the used TE-line is set to low (Registers, what are set by "Tearing Effect Line On (35h)" command, are keeping their current values) when it can be reactivated by "Tearing Effect Line On (35h)" command.

The flow chart for this internal function is following:



NOTES:

- 1. There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DCh), by the display module.
- 2. This information is only used if TE line is used.

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5.13.2 Functionality Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of these commands is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by "Tearing Effect Line On (35h)" command, are keeping their current values) when it can be reactivated by "Tearing Effect Line On (35h)" command.

The flow chart for this internal function is following:



NOTES:

- 1. There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.
- 2. This information is only used if TE line is used.

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5.13.3 Chip Attachment Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by "Tearing Effect Line On (35h)" command, are keeping their current values) when it can be reactivated by "Tearing Effect Line On (35h)" command.

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



NOTE: This information is only used if TE line is used.

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5.14 Display Panel Color Characteristics

Color characteristics of the display panel are stored on the display module that they can be read via the used interface by the engine what is using this display panel color characteristics information to adjust a color information of the image frame, what is on the engine, to match a wanted color outlook of the image on the display panel.

Used color characteristics can share 2 categories: Mandatory and Optional. The mandatory color characteristics are Black, White, Red, Green and Blue. The optional color characteristics is used if it is needed and it is called as A color (e.g. Cyan). The bits of the A color are set to '0's they are not used on the display module.

A read color characteristic value is based on 10 bit floating value where the MSB is 9th bit and the LSB is 0th bit. All power values of the bits are listed below:

- Bit 9: 2-1 = 0.5,
- Bit 8: 2-2 = 0.25,
- Bit 7: 2-3 = 0.125,
- Bit 6: 2 4 = 0.0625,
- Bit 5: 2-5 = 0.03125,
- Bit 4: 2-6 = 0.015625,
- Bit 3: 2-7 = 0.007813,
- Bit 2: 2-8 = 0.003906,
- Bit 1: 2-9 = 0.001953,
- Bit 0: 2-10 = 0.000977.

The wanted value is an approximation in the most of the cases when there is used binary numbers. Therefore, there is used the nearest value what can get e.g. Rx can be:

- Actual value: 0.6400, Stored value Rx[9:0] = 10 1000 1111b = 0.6396,
- Actual value: 0.3300, Stored value Rx[9:0] = 01.0101 0010b = 0.3301,
- Actual value: 0.3000, Stored value Rx[9:0] = 01 0011 0011b = 0.2998,
- Actual value: 0.6000, Stored value Rx[9:0] = 10 0110 0101b = 0.5986,
- Actual value: 0.1500, Stored value Rx[9:0] = 00 1001 1010b = 0.1504,
- Actual value: 0.0600, Stored value Rx[9:0] = 00 0011 1101b = 0.0596,
- Actual value: 0.3127, Stored value Rx[9:0] = 01 0100 0000b = 0.3125,
- Actual value: 0.3290, Stored value Rx[9:0] = 01 0101 0001b = 0.3291.

The value 0.6396 has calculated as follows:

- Binary value: 10 1000 1111b
- Formula: Rx[9]x0.5+Rx[8]x0.25+Rx[7]x0.125+Rx[6]x0.0625+Rx[5]x0.03125+Rx[4]x0.015625+Rx[3]x0.007813+Rx[2]x0.003906+Rx[1]x0.001953+R[0]x0.000977
- Use: 1x0.5+0x0.25+1x0.125+0x0.0625+0x0.03125+0x0.015625+1x0.007813+1x0.003906+ 1x0.001953+1x0.000977

See also sections:

"Read Black/White Low Bits (70h)", "Read Bkx (71h)", "Read Bky (72h)", "Read Wx (73h)", "Read Wy (74h)", "Read Red/Green Low bits (75h)", "Read Rx (76h)", "Read Ry (77h)", "Read Gx (78h)", "Read Gy (79h)", "Read Blue/AColor Low Bits (7Ah)", "Read Bx (7Bh)", "Read By (7Ch)", "Read Ax (7Dh)", "Read Ay (7Eh)".

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5.15 Gamma Function

The structure of grayscale amplifier is shown as below. The 26 voltage levels between VGMP and VGSP are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



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5.16 Basic Display Mode

The NT35510 has some basic operation modes which are Normal Display Mode, Partial Display Mode, Idle Mode, All Pixel On and All pixel Off for panel display. User can change these display modes for each other is illustrated below.



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5.17 Instruction Setting Sequence

When setting instruction to the NT35510, the sequences shown in below figures must be followed to complete the instruction setting.

5.17.1 Sleep In/Out Sequence



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5.17.2 Deep Standby Mode Enter/Exit Sequence





5.18 Instruction Setup Flow

5.18.1 Initializing with the Built-in Power Supply Circuits



Fig. 5.18.1 Initializing with the built-in power supply circuit

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initializing.

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5.18.2 Power OFF Sequence



Fig. 5.18.2 Power off sequence



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5.19 MTP Write Sequence Start Power on and normal display RDMTP command Check related End MTP_STUS1 bit = 0 (EF00h) MTP_STUS2 bit = 0 (EF01h) MTP was programmed Yes Adjust the MTP registers to optimal value * Refer command EDxxh for the related MTP registers MTPEN command (ED00h, ED01h) Set related MTP_EN1 bit = 1 MTP Connect high voltage 7.75V to MTP_PWR pin Programming 7.75V is not connected to MTP_PWR pin MTPDET command (EC00h) Check MTP DET bit = 1 No Yes MTPWR command (EE00h) Wait for more than 500 msec Remove high voltage 7.75V from MTP_PWR pin MTPEN command (ED00h, ED01h) Set all MTP_EN1 bit = 0 Set hardware reset SLPOUT command (1100h) MTP Programming Verify Read MTP registers all correct ? Re-execute MTP Programming Sequence Yes End

Note: The multi-times MTP must be programmed from the 1st time. (ID1/2/3, VGMP/VGSP, VGMN/VGSN, VCOM, Gamma 2.2, VGMP/VGSP LUT)

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5.20 Column, 1-Dot, 2-Dot, 3-Dot and 4-Dot Inversion (VCOM DC Drive)

The NT35510, in addition to the frame-inversion liquid crystal drive, supports the column, 1–dot, 2-dot, 3-dot and 4-dot inversion driving methods to invert the polarity of liquid crystal. The column, 1–dot, 2-dot, 3-dot and 4-dot inversion can provide a solution for improving display quality.

In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel. Note that setting 1-dot inversion will raise the frequency of the liquid crystal polarity inversion and increase the charging/discharging current on liquid crystal cells.

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6 COMMAND DESCRIPTIONS

6.1 User Command Set

	107	-	Ad	dress			Pa	ramete	er					_
Instruction	ACT	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOP	Dir	w	00h	0000h		No Ai	gument	(0000h	in MDDI	I/F)				No Operation
SWRESET	Cnd1	w	01h	0100h			gument							Software reset
				0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID
RDDID	Dir	R	04h	0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
				0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
RDNUMPE	Dir	R	05h	х	х	P7	P6	P5	P4	P3	P2	P1	P0	Read No. of the Errors on DSI only
RDDPM	Dir	R	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Power Mode
RDDMADCTL	Dir	R	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display MADCTR
RDDCOLMOD	Dir	R	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	DO	Read Display Pixel Format
RDDIM	Dir	R	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Image Mode
RDDSM	Dir	R	0Eh	0E00h	00h	D7	D6	D5 🧹	D4	D3	D2	D1	DO	Read Display Signal Mode
RDDSDR	Dir	R	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Self-diagnostic result
SLPIN	DVS	w	10h	1000h		No Ar	gument	(0000h	in MDDI	I/F)			/	Sleep in & booster off
SLPOUT	Dir	w	11h	1100h	\langle		gument				_	7	ĬC.	Sleep out & booster on
PTLON	DVS	w	12h	1200h		No Ai	gument	(0000h	in MDDI	I/F)			117	Partial mode on
NORON	DVS	w	13h	1300h		No Ar	gument	(0000h	in MDDI	1/E)		.//	<u>)) ((</u>	Partial off (Normal)
INVOFF	DVS	w	20h	2000h			gument		- 11	11			9	Display inversion off (normal)
INVON	DVS	w	21h	2100h			gument			- 11				Display inversion on
ALLPOFE	DVS	w	22h	2200h			gument							All pixel off (black)
ALLPON	DVS	w	23h	2300h		-	gument							All pixel on (white)
GAMSET	DVS	w	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Gamma curve select
DISPOFF	DVS	w	28h	2800h		No Ar	rgument	(0000h	in MDDI	I/F)				Display off
DISPON	DVS	w	29h	2900h			gument							Display on
				2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	Column address set
				2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	XS[15:0]: column start address XE[15:0]: column end address
CASET	Dir	w	2Ah	2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
				2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
				2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Row address set
				2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	YS[15:0]: row start address YE[15:0]: row end address
RASET	Dir	w	2Bh	2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
				2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
RAMWR	Dir	w	2Ch	X	X	D7	D6	D5	D4	D3	D2	D1	D0	Memory write
RAMRD	Dir	R	2Eh	2E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read
				3000h	00h	PSL15					PSL10	PSL9	PSL8	Partial start/end address set
				3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	PSL[15:0]: partial start address PEL[15:0]: partial end address
PTLAR	DVS	W	30h	3002h	00h	PEL15					PEL10	PEL9	PEL8	
				3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3		PEL1	PEL0	
TEOFF	DVS	w	34h	3400h			gument					=.		Tearing effect line off
TEON	DVS	w	35h	3500h	00h	-	-	-	-	-	-	-	м	Tearing effect mode set & on
MADCTL	Cnd2	w	36h	3600h	00h	MY	мх	MV	ML	RGB	мн	RSMX	RSMY	Memory data access control
IDMOFF	DVS	w	38h	3800h			gument	1						Idle mode off
.5	2.00	w	0.011	000011			gument			,				Idle mode on

Table 6.1.1 User Command Set

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Table 6.1.1 User Command Set (Continued)																
Instruction	АСТ	R/W	Ad	dress			Pa	ramete	er					Function		
matraction	701		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
COLMOD	Dir	w	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	Interface pixel format		
RAMWRC	Dir	w	3Ch	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory write Continue		
RAMRDC	Dir	R	3Eh	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read Continue		
STESL	DVS	w	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line		
STESL	DV5	vv	441	4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0			
			45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line		
GSL	Dir	R	45h	4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0			
DSTBON	DVS	w	4Fh	4F00h	00h	0	0	0	0	0	0	0	DSTB	Deep standby mode on		
				5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010	Write profile value for display		
				5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020			
WRPFD	DVS	w	50h	:	:	:	:	:	:	:	:	7	2			
				500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150			
				500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160			
WRDISBV	DVS	w	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness		
RDDISBV	Dir	R	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness value		
WRCTRLD	DVS	w	53h	5300h	00h	0	0	BCTRL	А	DD	BL	DB	G	Write control display		
RDCTRLD	Dir	R	54h	5400h	00h	0	0	BCTRL	A	DD	BL	DB	G	Read control display value		
WRCABC	DVS	w	55h	5500h	00h	0	0	0	0	0	0	C 1	CO	Write CABC mode		
RDCABC	Dir	R	56h	5600h	00h	0	0	0	0	0	0	C1	CO	Read CABC mode		
			5	5700h	00h	1017	1016	1015	1014	1013	1012	1011	1010	Write hysteresis		
				5701h	00h	1027	1026	1025	1024	1023	1022	1021	1020			
6								\mathbf{C}	//	ר ה		:	:	:	:	
	NN			570Eh	00h	1157	1156	1155	1154	1153	1152	1151	l150			
MMA))	S.		570Fh	00h	1167	1166	l165	l164	1163	1162	1161	l160			
WRHYSTE	DVS	w	57h	5710h	ooh	D017	D016	D015	D014	D013	D012	D011	D010			
11 ~				5711h	00h	D027	D026	D025	D024	D023	D022	D021	D020			
				UN I	:	:	:	:	:	:	:	:	:			
				571Eh	00h	D157	D156	D155	D154	D153	D152	D151	D150			
				571Fh	00h	D167	D166	D165	D164	D163	D162	D161	D160			
				5800h	00h	G023	G022	G021	G020	G013	G012	G011	G010	Write gamma setting		
				5801h	00h	G043	G042	G041	G040	G033	G032	G031	G030			
WRGAMMSET	DVS	w	58h	:	:	:	:	:	:	:	:	:	:			
				5806h	00h	G143	G142		G140	G133	G132	G131	G130			
				5807h	00h	G163	G162	G161	G160	G153	G152	G151	G150			
RDFSVM	Dir	R	5Ah	5A00h	00h			FSV13			FSV10	FSV9	FSV8	Read FS value MSBs		
RDFSVL	Dir	R	5Bh	5B00h	00h	FSV7	FSV6	FSV5		FSV3	FSV2	FSV1	FSV0	Read FS value LSBs		
RDMFFSVM	Dir	R	5Ch	5C00h	00h			FSV5						Read redian filter FS value MSBs		
RDMFFSVM		R	5Dh	5D00h	00h			FFSV13				FFSV9	FFSV0			
	Dir															
WRCABCMB	DVS	W	5Eh	5E00h	00h	CMB7	CMB6	CMB5		CMB3	CMB2	CMB1	CMB0	Write CABC minimum brightness		
RDCABCMB	Dir	R	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Read CABC minimum brightness		

Table 6.1.1 User Command Set (Continued)

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Table 6.1.1 User Command Set (Continued)														
Instruction	АСТ	R/W	Ad	dress			Pa	ramete	er	-	•			Function
moti dotion			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRLSCC	DVS	w	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Write light sensor compensation
WILLOOD	DV3	vv	0311	6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	coefficient
RDLSCCM	Dir	R	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Read LSCC value MSBs
RDLSCCL	Dir	R	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Read LSCC value LSBs
RDBWLB	Dir	R	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	Read Black/White low bit
RDBkx	Dir	R	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	Read Bkx
RDBky	Dir	R	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	Read Bky
RDWx	Dir	R	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	Read Wx 🔨 🚺
RDWy	Dir	R	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	Read Wy
RDRGLB	Dir	R	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	Read Red/Green low bit
RDRx	Dir	R	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Read Rx
RDRy	Dir	R	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	Read Ry
RDGx	Dir	R	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	Read Gx
RDGy	Dir	R	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	Read Gy
RDBALB	Dir	R	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	Read Blue/AColor low bit
RDBx	Dir	R	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	Read Bx
RDBy	Dir	R	7Ch	7C00h	00h	Ву9	By8	By7	By6	By5	By4	Ву3	By2	Read By
RDAx	Dir	R	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	Read Ax
RDAy	Dir	R	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	АуЗ	Ay2	Read Ay
		- 6	5	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB start
	2	11 11		A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
RDDDBS	Dir	R	A1h	A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
$\langle \rangle$	N_{Z}	91	1	A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
$J \ A$	ノ	\mathbf{v}		A104h	00h	1	1	1	1	1	1	1	1	
			0	A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB continue
V				A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
RDDDBC	Dir	R	A8h	A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A804h	00h	1	1	1	1	1	1	1	1	
RDFCS	Dir	R	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	Read first checksum
RDCCS	Dir	R	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	Read continue checksum
RDID1	Dir	R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
RDID2	Dir	R	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
RDID3	Dir	R	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Table 6.1.1 User Command Set (Continued)

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Notes:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line
4	Cnd1 (By Conditional 1)	StateExecuting timeWhen Sleep InDirOtherDHS
5	Cnd2 (By Conditional 2)	State Executing time B7, B6, B5 Dir B4, B3, B2, B1, B0 DVS

- 2. In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. See more information on the section "5.4 DATA TRANSFER RECOVERY". This note is valid when a number of the parameters is equal or less than 32 (In case of other interfaces, parameters of command 2A00h~2A03h are stored on relative registers while command 2A00h~2A03h are executed completely and same for command 2B00h~2B03h, 3000h~3003h and 4000h~4001h).
- 3. When using the commands without parameter (No Argument) in MDDI interface, a dummy parameter must be followed after command address. For example, command SPLOUT can be executed as 0x11 only in MIPI, MPU and SPI interfaces but should be executed as 0x1100 + 0x0000 in MDDI interface.



NOP (0000h)

Inst / Para	R/W	Add	ress				Parame	ter				
inol / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
NOP	Write	00h	0000h		No /	Argume	nt (0000	h in MD	DI I/F)			
DTE: "-" Don't car	е											
Description	Howe data r	ver it car ead cont	i be used inue as c	y command. It does no d to terminate RAM da described in RAMWR e) and RAMRDC (Me	ta writ (Memc	e, RAM ory Write	data rea e), RAM	ad, RAN RD (Me	l data w mory R	ead), RA	AMWRC	
Restriction	-											
Register Availability		Normal N Partial N	<i>l</i> ode On lode On, lode On,	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	Out Out			Av	ailability Yes Yes Yes Yes Yes			
Default Flow Chart			S	Status On Sequence W Reset W Reset			3	Deta	N/A N/A N/A N/A	Je		

Version 0.00



SWRESET: Software Reset (0100h)

Inst / Para	R/W	Add	ress			F	Parame	ter				
inst / rafa		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SWRESET	Write	01h	0100h		No A	Argumer	nt (0000	h in MD	DI I/F)			
DTE: "-" Don't care	9											
				set command is writt								ds an
Description	•			V Reset default value	s. (See	default I	ables ir	n each d	commar	nd descr	ription)	
				mediately. ory content is kept or	not by	this com	mand					
				vait 5msec before se				llowing	softwar	e reset		
			-	ids all display supplie	-			-				nsec.
Restriction				plied during Sleep Ou		-			-		-	
	•	Out con							191			2
	Softwa	are Rese	et comma	and cannot be sent du	uring Sl	eep Out	sequen	ice.	<u> </u>	<u> </u>		
									<u> </u>			
				Status				Av	ailability	/		
				, Idle Mode Off, Sleep					Yes	3		
Register				, Idle Mode On, Sleer	\cdots	U V		-	Yes			
Availability				Idle Mode Off, Sleep			11-		Yes Yes	~		
		Farliari	- 0 11	Idle Mode On, Sleep Sleep In	Out		2		Yes			
				Oleepin	<u>a (</u>				103			
1	TA	\\ \\										
\square		-						D -(
$n \cap N$		00	Dawa	Status				Deta	ault Valu	le		
Default		. (On Sequence W Reset					N/A N/A			
	5			/W Reset					N/A			
				i i i i i i i i i i i i i i i i i i i					1 1/7 1			
		1 23	<u> </u>									
		V	_					[Lege	nd		
			L	SWRESET(01h)				į	Logo			
							Host	- I	\sim	\neg		
				V	~		Driver	`¦[_(Comma	and		
			(Display whole blank screen)			¦/ī	Parame	$\frac{1}{1}$		
								·	urume			
Flow Chart			<i>_</i>	Set				$\left \right $	Displa	av) ¦		
riow on art				Command	\mathbf{i}							
			\langle	to S/W Default	\geq			_i<	Actio	<u> </u>		
			\backslash	Value	/				Mode			
			~	•						\leq		
			\bigcap	Sleep In Mode	\mathbf{r}				Sequer			
I												
			\sim		ノ				transf			

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RDDID: Read Display ID (0400h~0402h)

lpot / Dara		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
RDDID	Read	04h	0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
			0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
NOTE: "-" Don't car	e											
Description	The 1 The 2 The 3 <i>Note:</i>	st parame nd param rd param <i>Comma</i>	eter (ID1) eter (ID2) eter (ID3)	24-bit display identific): the module's manu !): the module/driver): the module/driver I D1/2/3 (DAh, DBh, I tively.	Ifacture version D.	ID. ID.		oond to	the pa	rameter	1, 2, 3	of the
Restriction	-		,				0	2 6	// //			
Register Availability		Normal N Partial N	<i>l</i> lode On lode On, lode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out o Out			AV	ailability Yes Yes Yes Yes Yes			
Default			J s	Status On Sequence /W Reset /W Reset	<u>ار</u>	MTP MTP	er MTP Values Values Values	ID ID	l=00h, l l=00h, l	ue efore MT D2=80h D2=80h D2=80h	, ID3=0 , ID3=0	0h
Flow Chart				RDDID(04h)	7 7 7]	Host Driver		Legen ommar aramete Display Action Mode equent transfe			

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last / D		Add	ress	-			Parame	ter				
Inst / Para	R/W	MIPI		D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDNUMED	Read	05h	Х	Х	P7	P6	P5	P4	P3	P2	P1	P0
NOTE: "-" Don't car	e											
Description	bits is P[60 P[7] is P[70 the firs See a	below.] bits are s set to "] bits are st param lso secti	e telling a 1" if there e set to " eter info on "Ackr	telling a number of the a number of the parity e is overflow with P[6 0"s (as well as RDDS rmation (= The read f nowledge with Error F for MIPI DSI only. It	v errors. 0] bits. SM(0Eh) function Report (<i>i</i>	's D0 ar is comp AwER)"	re set "C pleted). and cor)" at the	same ti RDDSM	ime) afte	·	
Restriction	-							2	<u> </u>	<u> </u>		
Register Availability		Normal I Partial N	Mode On Node On	Status I, Idle Mode Off, Slee I, Idle Mode On, Slee I, Idle Mode Off, Slee I, Idle Mode On, Slee Sleep In	p Out o Out			AV	railability Yes Yes Yes Yes Yes			
Default				Status On Sequence W Reset	ŋ			Defa	ault Valu 00h 00h 00h	ne		
Flow Chart			s	RDNUMED(05h) Gend 1 st Parameter P[7:0] = 00h DDSM(0Eh)'s D0='0	7		Hos Drive		Lege Comma Parame Displa Actio Mode Sequer transf	and eter ay n etial		

RDNUMED: Read Number of Errors on DSI (0500h)

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Inst / Para	R/W	Ade	dress				Parame	ter							
inst / Para	F7/ V V	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	DC			
RDDPM	Read	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	DC			
OTE: "-" Don't ca	ire									-					
	This c	omman	d indicate	s the current status o	of the di	splay as	s descril	oed in th	ne table	below:					
	E	Bit		Description				Val	lue						
)7	Booster V	oltage Status	"1"=	Booster	r On, "0'	'=Boost	er Off						
		06	Idle Mode	e On/Off	"1"=	Idle Mo	de On,	"0"=Idle	Mode (Off					
D				ode On/Off				-		I Mode (
Description			Sleep In/0			-				In Mode	<u> </u>				
				ormal Mode On/Off						play Noi	rmal Off	2			
			Display C		"1" = Display is On, "0" = Display is Off										
			Not Defin		Set to "0" (not used)										
		00	Not Defin	ed	Set to "0" (not used)										
Restriction	-														
				Status	Availability										
		Normal	Mode On	, Idle Mode Off, Slee	Out	6			Yes						
Register				, Idle Mode On, Slee			51		Yes						
Availability				Idle Mode Off, Sleep	-		$\overline{\mathbf{C}}$		Yes						
				Idle Mode On, Sleep					Yes						
		<u> </u>		Sleep In	Yes										
///))//		V				- ·									
	0			Status				ue							
Default		M	Power	On Sequence					08h						
		$\overline{(1, C)}$		/W Reset					08h						
		~	H	/W Reset					08h						
	<u> </u>														
								[]							
									egend						
			[RDDPM(0Ah)						1:					
							Host	Coi	mmand	_l;					
			~		7	Ľ	Driver		ameter	7					
			/ 5	Send 1 st Parameter	er /										
Flow Chart				/	Display										
Flow Chart															
								i < _	ction	>¦					
									Node						
						Sequentia									
									ansfer_	≤¦					
	1							L		1					

RDDPM: Read Display Power Mode (0A00h)

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Inst / Para	R/W	Ac	dress				Parame	ter						
inst / Para	R/W	W MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 D3 D2 D1 D0 ad 0Bh 0Booh 00h D7 D6 D5 D4 D3 D2 D1 D0 ad 0Bh 0Booh 00h D7 D6 D5 D4 D3 D2 D1 D0 s command indicates the current status of the display as described in the table below: Bit Description Value D7 Row Address Order (MY) "0" = Increment , "1" = Decrement												
RDDMADCTL	Read	ad 0Bh 0Booh 00h D7 D6 D5 D4 D3 D2 D1 D0 his command indicates the current status of the display as described in the table below: Bit Description Value D7 Row Address Order (MY) "0" = Increment, "1" = Decrement D6 Column Address Order (MX) "0" = Increment, "1" = Decrement D5 Row/Column Exchange (MV) "0" = Normal, "1" = Row/column exchange D4 Vertical refresh Order (ML) "0" = Increment, "1" = Decrement												
NOTE: "-" Don't cai	re													
			nd indicate		of the di	splay a	s descril	bed in th						
		-										200		
Description								-				iye		
Description		D3	RGB-BG	· · · ·			"0" = R	GB colo GR colo	r seque	ence		1		
		D2	Horizonta	al refresh Order (MH)			-			Decrem	nent			
		D1	Flip horiz	ontal (RSMX)	"0" = Normal, "1" = Horizontal flip									
		D0	Flip vertion	cal (RSMY)		"0" = Normal , "1" = Vertical flip								
Restriction	-				≥₩									
restriction		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes												
Register		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes												
Availability	n ^c						$\overline{\bigcirc}$		Yes					
10				, Idle Mode On, Sleep					Yes					
		0.0	5	Sleep In	J.				Yes					
		~	\sim											
		$\leq H$	$\left\{ \begin{array}{c} \end{array}\right\}$	Status		1	Default Value							
Default			Powe	r On Sequence				Don	00h					
Delault		\		S/W Reset					00h					
				I/W Reset					00h					
					1				egend					
			L.	RDDMADCTL(0Bh)				1	-	-1				
			Ľ				Host		mmand	li				
				••••••			Driver							
			[Send 1 st Parameter	7	_		i/ Par	ameter	_/¦				
			\sum						isplay	٦¦				
Flow Chart									ispiay	ノ				
		Action												
									\sim					
									quentia ansfer_	')i				
								⊥ <u> </u>		S i				
										1				

RDDMADCTL: Read Display MADCTL (0B00h)

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Version 0.00



Inst / Para	R/W	Ad	dress				Parame	ter				
inst / Para	H/VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDCOLMOD	Read	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0
IOTE: "-" Don't cai	re											
	This c	ommar	nd indicate	es the current status of	of the di	splay as	s descril	oed in th	ne table	below:		
		Bit		Description					Valu	е		
		07	Not Defin	ed				0" (not i	,			
		54		rface Color Format				16-bit /	•			
Description	D6	~ D4	RGD IIIle	nace Color Format				18-bit / 24-bit /	•	~	Π	
Booonplion	Г	03	Not Defin	ed				0" (not i				
		55	Not Denn					16-bit /		517/		
	D2	~ D0	Control Ir	nterface Color Forma	t			18-bit /		<u>\</u> U		
						25		24-bit /		U		
						2////		JU V				
Restriction	-									2		
									ット			
				Status				Av	ailability			
Register			XXX //	, Idle Mode Off, Slee	•		\mathbb{C}		Yes Yes			
Availability		Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out							Yes			
ſ	R		F	, Idle Mode On, Sleep	\cup			Yes				
				Sleep In					Yes			
	ΗĒ	V			<u> </u>							
	2			Status				Defa	ault Valu	Je		
Default		\overline{V}		On Sequence					07h			
		$\frac{1}{\sqrt{2}}$		W Reset					07h			
			F	I/W Reset					07h			
								r ·				
					1			I Le	egend	ļ		
			∏ F	RDDCOLMOD(0Ch)						7!		
					J		Host	Cor	nmand			
				▼	 	E	Driver					
			/ 9	Send 1 st Parameter	/			IZ Par	ameter	∠¦		
Flow Chart				/					isplay	٦!		
Flow Ghan												
						Action						
									/lode			
									_	∕		
									quentia ansfer_	')i		
										≤j		
	1							<u> </u>		1		

RDDCOLMOD: Read Display Pixel Format (0C00h)

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Version 0.00



RDDIM: Read Dis	piayi			Duun)										
Inst / Para	R/W	_	dress			1	Parame		_	_	_	_		
		MIPI		D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
	Read	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0		
NOTE: "-" Don't care					<i></i>									
	r	1	id indicate	es the current status o	of the	display as	s descril			below:				
		Bit D7	Vortical S	Description Scrolling On/Off		Set to "0'	' (not us		alue					
		D6		al Scrolling On/Off		Set to "0"								
		D5	Inversion	-		"1" = Inve			Inversio	on Off	~			
Description	-		All Pixel ("1" = Whi					/			
		03	All Pixel			"1" = Blad				N IN	$\sim \cdots$	1		
	D2	~ D0	Gamma	Curve Selection		"000" = 0 "010" = 0 "100" to "	GC0, " GC2, "	001" = 0 011" = 0	∋C1 ∋C3		110			
Restriction	-			~	TE LINE									
Register Availability Default		Normal Partial	Mode On Mode On Mode On Power	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep , Idle Mode On, Sleep Sleep In Status T On Sequence S/W Reset I/W Reset	3		ailability Yes Yes Yes Yes Yes ault Valu 00h 00h							
Flow Chart				RDDIM(0Dh)] 7		Host Priver		egend mmand rameter isplay action Mode quential ansfer	> > >				

RDDIM: Read Display Image Mode (0D00h)

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Version 0.00



Inst / Para R/W Number of the status of the	t is "0"								
IOTE: "-" Don't care This command indicates the current status of the display as described in the table be Bit Description Value D7 Tearing Effect Line On/Off "1" = On, "0" = Off D6 Tearing Effect Line Mode "1" = Mode 2, "0" = Mode 1 D5 Horizontal Sync. (HS, RGB I/F)On/Off "1" = HS bit is "1", "0" = HS bit D4 Vertical Sync. (VS, RGB I/F)On/Off "1" = PCLK line is On, "0" = PC D2 Data Enable (DE, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI ("1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been Yes Register Normal Mode On, Idle Mode Off, Sleep Out Yes Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Yes	elow: t is "0" t is "0"								
This command indicates the current status of the display as described in the table be Bit Description Value D7 Tearing Effect Line On/Off "1" = On, "0" = Off D6 Tearing Effect Line Mode "1" = Mode 2, "0" = Mode 1 D5 Horizontal Sync. (HS, RGB I/F)On/Off "1" = HS bit is "1", "0" = HS bit D4 Vertical Sync. (VS, RGB I/F)On/Off "1" = PCLK line is On, "0" = PC D3 Pixel Clock (PCLK, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Erron, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this command has been and the status of the lines when this co	t is "0"								
BitDescriptionValueD7Tearing Effect Line On/Off"1" = On, "0" = OffD6Tearing Effect Line Mode"1" = Mode 2, "0" = Mode 1D5Horizontal Sync. (HS, RGB I/F)On/Off"1" = HS bit is "1", "0" = HS bitD4Vertical Sync. (VS, RGB I/F)On/Off"1" = VS bit is "1", "0" = VS bitD3Pixel Clock (PCLK, RGB I/F)On/Off"1" = PCLK line is On, "0" = PCD2Data Enable (DE, RGB I/F)On/Off"1" = DE bit is "1", "0" = DE bitD1Not DefinedSet to "0" (not used)D0Error on DSI"1" = Error, "0" = No ErrorNote: Bit D5 to D2 indicate current status of the lines when this command has been and the status of the lines when this command has been and	t is "0"								
Big D7 Tearing Effect Line On/Off "1" = On, "0" = Off D6 Tearing Effect Line Mode "1" = Mode 2, "0" = Mode 1 D5 Horizontal Sync. (HS, RGB I/F)On/Off "1" = HS bit is "1", "0" = HS bit D4 Vertical Sync. (VS, RGB I/F)On/Off "1" = VS bit is "1", "0" = HS bit D3 Pixel Clock (PCLK, RGB I/F)On/Off "1" = PCLK line is On, "0" = PCLK D2 Data Enable (DE, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been and the status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes	t is "0"								
D6 Tearing Effect Line Mode "1" = Mode 2, "0" = Mode 1 D5 Horizontal Sync. (HS, RGB I/F)On/Off "1" = HS bit is "1", "0" = HS bit D4 Vertical Sync. (VS, RGB I/F)On/Off "1" = VS bit is "1", "0" = VS bit D3 Pixel Clock (PCLK, RGB I/F)On/Off "1" = PCLK line is On, "0" = PCLK D2 Data Enable (DE, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been and the lines the lines when this com	t is "0"								
Description D5 Horizontal Sync. (HS, RGB I/F)On/Off "1" = HS bit is "1", "0" = HS bit D4 Vertical Sync. (VS, RGB I/F)On/Off "1" = VS bit is "1", "0" = VS bit D3 Pixel Clock (PCLK, RGB I/F)On/Off "1" = PCLK line is On, "0" = PC D2 Data Enable (DE, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes	t is "0"								
Description D4 Vertical Sync. (VS, RGB I/F)On/Off "1" = VS bit is "1", "0" = VS bit D3 Pixel Clock (PCLK, RGB I/F)On/Off "1" = PCLK line is On, "0" = PCLK D2 Data Enable (DE, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been and the status Availability Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes	t is "0"								
D3 Pixel Clock (PCLK, RGB I/F)On/Off "1" = PCLK line is On, "0" = PCD2 D2 Data Enable (DE, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been and the status Availability Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes									
D2 Data Enable (DE, RGB I/F)On/Off "1" = DE bit is "1", "0" = DE bit D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been to be indicate current status of the lines when this command has been to be indicate current status of the lines when this command has been to be indicate current status of the lines when this command has been to be indicate current status of the lines when this command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the command has been to be indicate current status of the lines when the current status of the l									
D1 Not Defined Set to "0" (not used) D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been and the lines when this command has been and the lines when this command has been and the lines when th									
D0 Error on DSI "1" = Error, "0" = No Error Note: Bit D5 to D2 indicate current status of the lines when this command has been and the lines when this command has been and the lines when the lines when the lines when the command has been and the lines when the lines when the command has been and the lines when the command has been and the lines when the	t is "0"								
Interview of the lines when this command has been in the lines when the l									
Restriction - Register Availability Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes									
Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes	sent.								
Register Normal Mode On, Idle Mode Off, Sleep Out Yes Availability Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes									
Register Normal Mode On, Idle Mode Off, Sleep Out Yes Availability Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes									
Register Normal Mode On, Idle Mode On, Sleep Out Yes Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes									
Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes									
Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes									
Sleep In Yes									
Status Default Value									
Default Power On Sequence 00h									
S/W Reset 00h									
H/W Reset 00h									
Legend									
	i								
RDDSM(0Eh) Host Command									
Driver / Parameter /	7¦								
Send 1 st Parameter									
Flow Chart Display	Display								
Action	Action								
Mode									
Sequential	,i								
transfer	<u>기</u>								
	-1								

RDDSM: Read Display Signal Mode (0E00h)

11/8/2010

Version 0.00



Inst / Para	B/W	Ad	dress				Parame	ter							
IIISt / Pala	n/ VV						D5	D4	D3	D2	D1	D			
RDDSDR	Read	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D			
OTE: "-" Don't ca	re														
	This c	ommar	id indicate	es the current status of	of the dis	splay as	s descril	oed in th	ne table	below:					
	E	Bit							Value						
)7		Loading Detection											
	-			ality Detection		See	section	5.13							
		05	-	chment Detection						~	Π				
Description		04		alass Break Detection	1		"O" (-	<u>a IN</u>					
			Not Defin			-	o "0" (n	<u> </u>							
			Not Defin			-	:o "0" (n								
		D1	Not Defin	ed		_	o "0" (n								
		00	Checksur	ns Comparison					the san						
Postriation				~		"1": Checksums are not the same									
Restriction	-					FILE									
				Status	121	Availability									
		Normal	Mode On	, Idle Mode Off, Sleep					Yes						
Register				, Idle Mode On, Slee					Yes						
Availability									Yes						
1		Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out							Yes						
		00	5	Sleep In	<u> </u>				Yes						
			≈ 1												
		<u></u>			Default Value										
V ~				Status		Default Value									
Default		$\ Z\ $		On Sequence		00h									
		U		S/W Reset					00h						
			F	I/W Reset					00h						
								,							
					1			i Lo	egend						
				RDDSDR(0Fh)				 		-1					
			L		J		Host		mmand	li					
				••••••	•••••	г	Driver			;					
			[Cond 1 st Paramotor	7	_		i/ Par	ameter	/¦					
	Send 1 st Parameter								· · · ·	\neg					
Flow Chart															
								$ \langle A$	ction	>!					
								j 🖊	/lode	ノ					
									quentia	\sim					
	1							IV tr	ansfer_	ニ					
								i ~~		≤¦					

RDDSDR: Read Display Self-Diagnostic Result (0F00h)

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SLPIN: Sleep In (1000h)

Inst / Para	R/W	Add	ress					Parame	ter			_			
liist / i ala	11/11	MIPI	Others	D[15:8] (Non-N	/IPI)	D7	D6	D5	D4	D3	D2		D1		D0
SLPIN	Write	10h	1000h			No /	Argumei	nt (0000	h in ME	DI I/F)					
OTE: "-" Don't ca	re														
Description	This c In this stoppe	mode the ed. Sou Memo In DC	ne DC/DC nrce / Ga ory Scar ternal O C / DC C nce as wil	onverter I as memory ar	opped, Bla	Intern	al displa	stc	ator is s	topped	, and pa				
	User of this in Sleep Dimm There	can send formatio Out-mo ing funct is used	d PCLK, H n is valic de. tion does an intern	ts contents. HS and VS infor d during 2 fram not work when al oscillator for	es afte there i blank o	er Slee is char display	ep In co nging mo	mmand ode fron	if there	e is use Out to	d Norn Sleep I	nal n.	Mod	e Or	n
Restriction	the Slo It will voltag It will	eep Out be nece es and c be nece:	Commar essary to clock circl	wait 5msec be uits to stabilize. vait 120msec a	fore so	ending	next co	ommano	d, this i	s to alle	ow time	e fo	or the	sup	рр
		<u> </u>		Status			T		Δ.,	ailabilit					-
		Normal	Mode On	Idle Mode Off,	Sleen	Out			AV	ailabilit Yes	у				_
Register				, Idle Mode On,			+			Yes					_
Availability				Idle Mode Off,			1			Yes					
			,	Idle Mode On,						Yes					٦
			,	Sleep In						Yes					
Default				Status On Sequence /W Reset					Slee	ault Val p In Mo p In Mo	de				





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SLPOUT: Sleep Out (1100h)

		Add	ress					Parame	ter				
Inst / Para	R/W	MIPI		D[15:8] (No	on-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	Write	11h	1100h		/	No	Argumer	nt (0000	h in MC	DI I/F)			
NOTE: "-" Don't car							0	(/			
Description	This c In this started	Memory Inte DC / can start node in N	e DC/DC e / Gate y Scan C rnal Osc DC Cor to send valid at le lormal Me		is enabled STOP STOP STOP and VS in before	ST	tion on F Out com	(II	f DISPOI	Blank N 29h is	CDP of Memory set)	or Frame (Contents	nd this
Restriction	Sleep reset. It will voltag NT355 there same NT355 It will	Out Mo be nece es and c 510 load cannot b when thi 510 is do be neces	de can o ssary to clock circe s all deta be any ab is load is ting self-o ssary to v	nce control nly be exit i wait 5msec uits to stabil ult values c normal visu done and w diagnostic fu wait 120mse an be sent.	by the Sl before s ize. If extended al effect of then the N unctions c	eep In sending ed and on the NT355 ⁻ luring t	Comma g next co test com display i 10 is alre his 5mse	ommand ommand to mage if ady Sle ec. See), S/W d, this is o the re those c ep Out also see	reset co s to allo gisters default a -mode. ction 5.	ow time during t and regis	for the his 5ms ster valu	supply ec and les are
				Status					Av	ailability	ý		
		Normal N	Node On	Idle Mode	Off, Sleep	o Out				Yes			
Register				Idle Mode						Yes			
Availability		Partial N	lode On,	Idle Mode (Off, Sleep	Out				Yes			
		Partial N	lode On,	Idle Mode (On, Sleep	Out				Yes			
				Sleep In						Yes			
Default			S	Status On Sequen /W Reset	ice				Slee Slee	ault Valı p In Mo p In Mo	de de		
			H	/W Reset					2166	p In Mo	ue]

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Inst / Para	R/W	Add	ress				Parame	ter				
inst / Para	Fi/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D
PTLON	Write	12h	1200h		No /	Argumer	nt (0000)h in MD	DDI I/F)			
)TE: "-" Don't car	e											
Description	comm To lea	and (30I ve Partia	H) al mode,	on Partial mode. Th the Normal Display M isual effect during mo	lode O	n comm	and (13	H) shou	ıld be w	ritten.		
Restriction	This c	ommano	has no	effect when Partial Di	splay n	node is a	active.					
Register Availability	1	Normal N Partial N	<i>l</i> lode On, lode On, lode On,	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	Out Out			Av	ailability Yes Yes Yes Yes Yes			
Default Flow Chart	See P	artial Ar	S	Status On Sequence W Reset /W Reset			3	Norm: Norm:	ault Valu al Mode al Mode al Mode	On On		

PTLON: Partial Display Mode On (1200h)

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NORON: Normal Display Mode On (1300h)

Inst / Para	R/W	Add	ress				Parame	ter						
liist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
NORON	Write	13h	1300h		No /	Argume	nt (0000	h in MD	DI I/F)					
OTE: "-" Don't car	e													
Description	Norma Exit fre	al display om NOR	v mode o ON by th	the display to normal n means Partial mode ne Partial mode On co isual effect during mo	e off. omman	• •	n Partia	l mode	On to N	lormal n	node Or	I.		
Restriction	This c	ommand	has no	effect when Normal D	isplay	mode is	active.							
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesSleep InYesYesYes												
Default Flow Chart	See P	Partial Are	S H	Status On Sequence /W Reset /W Reset	letails o	of when	to use t	Norma Norma Norma	ault Valu al Mode al Mode al Mode mand	On On				

Version 0.00



INVOFF: Display Inversion Off (2000h)

lpot / Dave	DAA	Add	ress			ł	Parame	ter				
Inst / Para	R/W	MIPI		D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
INVOFF	Write	20h	2000h		No	Argumer	nt (0000	h in MD	DI I/F)		_	
IOTE: "-" Don't car	е											
Description	This c	ommano ommano	d makes i d does no	to recover from disp no change of conten of change any other s	ts of fra			Display			Π	
Description												1
Restriction	This c	ommano	has no	effect when module	is alread	ly in Inve	ersion C)ff mode	э.	1		
Register Availability		Normal N Partial N	Aode On, Iode On, Iode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out p Out		3	Av	ailability Yes Yes Yes Yes Yes			
Default			S S	Status On Sequence /W Reset /W Reset				Display Display	ault Valu Inversio Inversio Inversio	on off on off		
Flow Chart				isplay Inversion On Mode INVOFF(20h) isplay Inversion Off Mode)				ommar ommar aramet Display Action Mode equent transfe			

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INVON: Display Inversion On (2100h)

Inst / Para	R/W	Add	lress			F	Parame	ter				
inst / Para	H/ VV	MIPI		D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
INVON	Write	21h	2100h		No /	Argumer	nt (0000	h in MD	DI I/F)			
OTE: "-" Don't car	e											
	This c	ommano	d makes	to enter display inver no change of content ot change any other s	s of frai		ory.					
				version On, the Displa		sion Off	comma	and (20h	n) shoul	d be wri	itten.	
	(Exam			Memory		0.011 0.1		Display	., ee.a.			
Description												2
Restriction	This c	ommano	d has no	effect when module is	s alread	ly in Inve	ersion C	n mode	Э.	1		
										1		
				Status				Av	ailability			
		Normal I	Mode On	, Idle Mode Off, Sleep	o Out	6	all	111	Yes			
Register				, Idle Mode On, Sleep		$\gamma \sim$	51		Yes			
Availability		Partial A	Aode On,	Idle Mode Off, Sleep	Out		\mathcal{I}		Yes			
		Partial N	lode On,	Idle Mode On, Sleep	o Out				Yes			
				Sleep In	ノビ				Yes			
<u> </u>	jΰ		<u> </u>									
		10	\mathcal{A}	Status				Defa	ault Valu	le		
Default	Ţ,	1111/2	Power	On Sequence					Inversio			
201001		\overline{U}		/W Reset					Inversio			
		U	Н	/W Reset				Display	Inversio	on off		
								[]	Legen			
				isplay Inversion	\mathbf{N}			į '	Logon			
			(Off Mode)							
			\sim		/				ommar	id i		
								¦/Ρ	aramete	er 7		
			_									
Flow Chart				INVON(21h)					Display			
				V				\leq	Action	>		
			(D	isplay Inversion)				Mode			
			\sim	On Mode	/				\sim			
									equent			
									transfe	r		
								L		!		

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ALLPOFF: All Pixel Off (2200h)

	Inst / Para	R/W	Add	lress				Parame	ter				
	llist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
	ALLPOFF	Write	22h	2200h		No /	Argumei	nt (0000	h in MC	DI I/F)			
1	NOTE: "-" Don't car	re											
	Description	registe This c This c "All Pi The d	er can be ommand ommand xels On" isplay pa	e on or of d makes i d does no Mer	he display panel blac f. no change of contents of change any other st nory	s of fran tatus.	ne mem	nory.	Display	(E s are us	xample sed to le) pave this	mode.
	Restriction	This c	ommano	d has no	effect when module is	alread	ly in All	Pixel Of	f mode.	3			
1	Register Availability		Normal N Partial N	Mode On, Iode On, Iode On,	Status Idle Mode Off, Sleep Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	Out Out		2	Av	ailability Yes Yes Yes Yes Yes	y		
	Default			S	Status On Sequence /W Reset /W Reset				All All	ault Vali pixel of pixel of pixel of	íf íf		





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ALLPON: All Pixel On (2300h)

Inst / Para	R/W	Add	ress				Parame	ter					
iiisi / Faia		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
ALLPON	Write	23h	2300h		No	Argumei	nt (0000	h in MD	DI I/F)				
OTE: "-" Don't car	e												
Description	registe This c This c (Exam "All Pi The d	er can be ommanc ommanc iple) xels Off"	e on or of I makes in I does no I does no	he display panel whit if. no change of contents of change any other sta Memory I Display Mode On" or nowing the content of	of fran atus.	me mem	nory.				eave this	s mode	
Restriction	This c	ommanc	has no	effect when module is	alread	ly in all I	Pixel Or	n mode.					
Register Availability		Normal N Partial N	<i>l</i> lode On lode On, lode On,		Out Out			Av	ailabilit Yes Yes Yes Yes Yes	у			
Default													

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GAMSET: Gamma Set (2600h)

	Add	Iress				Parame	ter						
Inst / Para F	R/W MIPI		D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMSET V	Vrite 26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		
OTE: "-" Don't care								0					
Т	This comman	d is use	d to select the desir	ed Garr	nma cur	ve for t	he curr	ent disp	olay. A r	naximu	m of 4		
			ed. The curve is se	lected	by setti	ng the	appropr	riate bit	in the	parame	eter as		
d	lescribed in t		1	-						_			
	GC[7:	0]	Parameter				Select						
Description	01h		GC0		Ga	amma C		G=2.2)		-			
-	02h		GC1				served		A h				
	04h 08h		GC2 GC3				served				2		
			are undefined.			RE	served	H		UP			
			shown in table above	o oro in	ulid on		tahana	o tho ou	rront oo	lootod o	ommo		
Restriction	curve until val			e are inv			cenany		inent se	lected g	amma		
				TIL					3				
			Status				Av	ailability					
	Normal	Mode On	, Idle Mode Off, Slee	n Out		n	TIL	Yes					
Register					6	$\gg \parallel$		Yes					
Availability		Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Yes											
			Idle Mode On, Slee	~		J		Yes					
	N II A		Sleep In					Yes					
				テレ									
					<u> </u>								
			Status				Defa	ault Valu	le				
Default			On Sequence					01h					
			S/W Reset					01h					
		Г	I/W Resel					01h					
						1							
						ļ	Le	egend					
								_					
		G	AMSET(26h)				Cor	mmand	li				
						į	001	manu	¦				
			V				Par	ameter	7:				
			GC[7:0]				\sim		<u> </u>				
Flow Chart						į		splay)¦				
			\bot										
							< A	ction	>;				
			lew Gamma			i		/lode	\supset				
			lew Gamma urve Loaded						$\sum_{i=1}^{n}$				
							Sec	quentia	$\sum_{i=1}^{n}$				
							Sec		$\sum_{i=1}^{n}$				

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DISPOFF: Display Off (2800h)

Inot / Dr		Add	ress			ł	Paramet	ter				
Inst / Para	R/W	MIPI		D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	Write	28h	2800h		No /	Argumer	nt (0000	h in MD	DI I/F)			
NOTE: "-" Don't car	e											
Description	disabl This c other (Exan	es and b command status. T nple)	lank pag d makes 'here will	to enter into DISPLAY e inserted. no change of conter be no abnormal visib Memory	nts of file effect	rame me	emory. T					-
Restriction	This c	ommano	has no	effect when module is	s alread	ly in Dis	olay Off	mode.		1		
Register Availability		Normal M Partial M	Mode On Node On, Node On, Power S	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode On, Sleep Idle Mode On, Sleep Sleep In Status On Sequence /W Reset	o Out Out			Defa Dis Dis	ailability Yes Yes Yes Yes Yes uult Valu play off play off	le		
Flow Chart				isplay On Mode DISPOFF(28h) isplay Off Mode)				egend ommar aramete Display Action Mode equent transfe			

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DISPON: Display On (2900h)

DISPON: Display		-	ress			F	arame	ter				
Inst / Para	R/W	MIPI		D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	Write	29h	2900h			Argumen						
NOTE: "-" Don't car						9	. (, . ,			
Description	This c This c	ommanc ommanc	d makes i d does no	to recover from DISF no change of content ot change any other s	s of fra		ory.	splay	Frame N	Memory	is enab	led.
Restriction	This c	ommano	has no	effect when module is	s alrea	dy in Disr	olay On	mode	V			
Register Availability Default		Normal M Partial M	Mode On, Node On, Mode On, Power S	Status , Idle Mode Off, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Idle Mode On, Sleep Sleep In Status On Sequence W Reset	o Out o Out			Defa Dis Dis	ailability Yes Yes Yes Yes ult Valu play off play off	Je f		
Flow Chart				isplay Off Mode DISPON(29h))				egen ommar aramet Display Action Mode equent transfe			

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CASET: Column Address Set (2A00h~2A03h)

Inst / Para	R/W	Add					Parame		1	T		•		
llist / T ala	10.00	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
			2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		
CACET	\\/wite	0.4 h	2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XSC		
CASET	Write	2Ah	2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		
			2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE		
NOTE: "-" Don't car	e													
	This c	ommand	d is used	to define area of frai	ne mer	ory whe	ere MPL	J can ac	cess.					
	This c	ommand	d makes	no change on the oth	ner drive	er status					Π			
	Each	value rep	oresents	one column line in th	ne Fram	e Memo	ory.			n M				
	(Exam	nple)		XS[15:0]	XE[15:0]]			151			2		
					Ļ	_		Ac	N N		DL			
Description							~ [[1 00				
						110			0					
						-				•				
						2 \\\								
		VS[15:0] always must be actual target loss than VE[15:0]												
	-	XS[15:0] always must be equal to or less than XE[15:0] When XS[15:0] or XE[15:0] is greater than maximum address like below, data of out of range will be												
)] or XE[15:0] is greater thar	n maxim	um add	ress lik	e below	, data d	of out of	range	will b		
	ignore		"701"		, N , I	()								
				480 x 864 resolution	· • • • • • • • • • • • • • • • • • • •		- 470 //							
				ange 0 ≦ XS[15:0] ange 0 ≦ XS[15:0]										
$\times \mathbb{N} (\mathbb{N} \setminus \mathbb{N} \setminus \mathbb{N})$				480 x 854 resolution	_	[15.0] ≧	≥ 003 (0	J35FII)						
		- //		ange $0 \leq XS[15:0]$		15:01 ≤	≤ 479 ((01DFh)						
				ange 0 \leq XS[15:0]	-	-								
Restriction				480 x 800 resolution			,	,						
	MV =	= "0": Pai	rameter i	range 0 \leq XS[15:0]	\leq XE[15:0] ≦	≦ 479 ((01DFh)						
				range 0 \leq XS[15:0]	-	[15:0] ≦	≦ 799 (0	031Fh)						
				480 x 720 resolution	,									
				ange 0 \leq XS[15:0]	-	-	•	,						
				ange 0 \leq XS[15:0]	-	[15:0] ≦	≦ /19 ((J2CFh)						
				480 x 640 resolution range 0 \leq XS[15:0]		15.01 <	- 170 ((
				ange 0 \leq XS[15:0] ange 0 \leq XS[15:0]										
	1010 -	- 1.14				10.0]	000 ((527111)						
				Status				Δν	ailability	1				
		Normal	Mode On	, Idle Mode Off, Slee	n Out			70	Yes	1				
Register				, Idle Mode On, Slee					Yes			-+		
Availability				Idle Mode Off, Slee	•				Yes			-+		
				Idle Mode On, Slee					Yes			-+		
				Sleep In	o Out				Yes					
						1			165					

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RASET: Row Address Set (2B00h~2B03h)

Inst / Para	R/W	Add	ress				Parame	ter				
ilist / i aia	11/99	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8
RASET	\\/wite	2Bh	2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
RASEI	Write	ZDII	2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8
			2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0
NOTE: "-" Don't car	e											
Description	This c	ommano value rep	I makes presents	to define area of fram no change on the oth one column line in th YS[15:0]	ner drive	r status		can ac	cess.			2
Restriction	When ignore For CO MV = For CO MV = For CO MV = For CO MV = For CO MV = For CO MV =	YS[15:C ed. GM[7:0] = "0": Pau = "1": Pau GM[7:0] = "0": Pau = "1": Pau GM[7:0] = "0": Pau GM[7:0] = "0": Pau GM[7:0] = "1": Pau GM[7:0] = "0": Pau)] or YE = "70h" (ameter (rameter (= "6Bh") rameter (ameter (ameter (ameter (ameter (cameter (cam	be equal to or less the [15:0] is greater than [15:0] is greater than [480 x 864 resolution range $0 \leq XS[15:0]$ range $0 \leq XS[15:0]$ (480 x 854 resolution range $0 \leq XS[15:0]$ (480 x 800 resolution range $0 \leq XS[15:0]$ range $0 \leq XS[15:0]$ (480 x 720 resolution range $0 \leq XS[15:0]$ range $0 \leq XS[15:0$	(maxim)	um add 15:0] ≦ 15:0] ≦ 15:0] ≦ 15:0] ≦ 15:0] ≦ 15:0] ≦ 15:0] ≦	 863 (0 479 (0 853 (0 479 (0 479 (0 799 (0 479 (0 719 (0 479 (0 639 (0)35Fh))1DFh))355h))1DFh))1DFh))1DFh))2CFh))1DFh))22Fh)	, data c	of out of	range	will be
Register Availability	I	Normal N	Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee	p Out			Av	ailability Yes Yes Yes			
		Partial M	lode On	, Idle Mode On, Sleep	o Out				Yes			
				Sleep In					Yes			

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RAMWR: Memory Write (2C00h)

Inst / Para	R/W	Add	ress				Parame	ter				
inst / i aia	11/99	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
RAMWR	Write	2Ch	2C00h	D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	DC
OTE: "-" Don't car	е											
Description	This c When Colum The S Then Sendi	ommand this co nn/Start I tart Colu D[23:0] i ng any o	d makes mmand Row pos Imn/Stari s stored ther com	t Row positions are d in frame memory and imand can stop Fram	er drive lumn re ifferent I the co ie Write	r status. egister a in accor lumn reg	and the dance v gister ar	row re vith MAI	egister a DCTL se ow regis	etting ter incre	emented	2
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode											
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes											
Default	Status Default Value Power On Sequence Contents of memory is set randomly SW Reset Contents of memory is set randomly H/W Reset Contents of memory is set randomly											
Flow Chart				AMWR(2Ch) Image Data 23:0], D2[23:0], , Dn[23:0]					egend mmano ramete Pisplay Action Mode quentia ransfer			

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RAMRD: Memory Read (2E00h)

Inst / Para	R/W	Add	ress				Parame	ter				
liist / Faia		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
RAMRD	Read	2Eh	2E00h	D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
OTE: "-" Don't car	е											
Description	This c When Colum The S Then incren	ommand this co nn/Start I tart Colu D[23:0] nented	d makes mmand Row pos Imn/Star is read	t Row positions are d back from the fram	er drive lumn re ifferent ne merr	r status. egister a in accor nory and	and the dance v d the co	row re vith MAI	egister a	etting.		2
Restriction	Frame Read can be canceled by sending any other command. There is no restriction on length of parameters. No access in the frame memory in Sleep In mode											
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes											
Default	Status Default Value Power On Sequence Contents of memory is set randomly SW Reset Contents of memory is set randomly H/W Reset Contents of memory is set randomly											
Flow Chart				RAMRD(2Eh) Image Data 23:0], D2[23:0], , Dn[23:0] ny Command					egend mmand ramete Display Action Mode			

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PTLAR: Partial Area (3000h~3003h)

Inst / Para		R/W Address Parameter MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 D3 D2 D1										
liist / T ala	R/W MIPI Others D[15:8] (Non-MIPI		D7	D6	D5	D4	D3	D2	D1	D0		
	Write		3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8
PTLAR		30h	3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0
	VVIIIC	0011	3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8
			3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0
NOTE: "-" Don't car	е											
Description	comm figures If End	and, the s below. Row > S Stari PSL End PEL End PEL Stari Row < S End PEL	first def PSL and Start Rov Row [15:0] [15:0] [15:0] [15:0] [15:0] [15:0] [15:0] [15:0] [15:0] [15:0] [15:0] [15:0] [15:0]	s the partial mode's ines the Start Row (F d PEL refer to the Fra v when MADCTL ML v when MADCTL ML	PSL) and ame Mer =0: Non-d Non-d F1: Non-d =0:	d the se mory row isplay Ar isplay Ar isplay Ar isplay Ar splay Ar	cond the v address ea ea ea ea ea	e End R ss coun	ow (PE ter.		ustratec	d in the

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	PSI [15:0] and PEI [15:0] about have below range	
Restriction		
Restriction CGM[7:0] = "6Bh" (480 x 854): 0 ≤ PSL[15:0], PEL[15:0] ≤ 853 (0355h), PEL-PSL CGM[7:0] = "50h" (480 x 800): 0 ≤ PSL[15:0], PEL[15:0] ≤ 799 (031Fh), PEL-PSL CGM[7:0] = "28h" (480 x 720): 0 ≤ PSL[15:0], PEL[15:0] ≤ 719 (02CFh), PEL-PSL CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-PSL CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-PSL CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-PSL Register Availability Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Status Pet[15:0] Default Value 035Fh (683d) if CGM 035Fh (683d) if CGM 027Fh (639d) if CGM 035Fh (633d) if CGM 027Fh (639d) if CGM 035Fh (683d) if CGM 027Fh (639d) if CGM 035Fh (663d) if CGM 027Fh (639d) if CGM 035Fh (663d) if CGM 027Fh (639d) if CGM 035Fh (663d) if CGM 035Fh (663d) if CGM 035Fh (663d) if CGM 027Fh (639d) if CGM 035Fh (663d) if CGM 027Fh (639d) if CGM		
	$CGM[7:0] = "00h" (480 \times 640): 0 \leq PSL[15:0], PE$	$L[15:0] \leq 639 (027Fh), PEL-PSL \leq 639 (027Fh)$
	Status	70h" (480 x 864): 0 \leq PSL[15:0], PEL[15:0] \leq 863 (035Fh), PEL-PSL \leq 863 (035Fh) 68h" (480 x 854): 0 \leq PSL[15:0], PEL[15:0] \leq 799 (031Fh), PEL-PSL \leq 799 (031Fh) 50h" (480 x 800): 0 \leq PSL[15:0], PEL[15:0] \leq 719 (02CFh), PEL-PSL \leq 719 (02CFh) 28h" (480 x 720): 0 \leq PSL[15:0], PEL[15:0] \leq 719 (02CFh), PEL-PSL \leq 639 (027Fh) 28h" (480 x 640): 0 \leq PSL[15:0], PEL[15:0] \leq 639 (027Fh), PEL-PSL \leq 639 (027Fh) Status Availability Mode On, Idle Mode Off, Sleep Out Yes 0000h 035Fh (863d) if CGM[7:0] = "70h" 035Fh (853d) if CGM[7:0] = "50h" 02CFh (719d) if CGM[7:0] = "6Bh" 0000h 035Fh (863d) if CGM[7:0] = "60h" 035Fh (863d) if CGM[7:0] = "60h" 035Fh (863d) if CGM[7:0] = "50h" 02Fh (399d) if CGM[7:0] = "50h" 02Fh (639d) if CGM[7:0] = "6Bh"
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
•	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
	Status	
		035Fh (863d) if CGM[7:0] = "70h"
		0355h (853d) if CGM[7:0] = "6Bh"
		031Fh (799d) if CGM[7:0] = "50h"
	Power On Sequence	02CFh (719d) if CGM[7:0] = "28h"
	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Status PEL[15:0] PEL[15:0] Power On Sequence 0000h 035Fh (863d) if CGM[7:0] = 0000h 027Fh (639d) if CGM[7:0] = 0355h (853d) if CGM[7:0] = SW Reset 0000h 035Fh (863d) if CGM[7:0] = 027Fh (639d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 027Fh (639d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 035Fh (863d) if CGM[7:0] = 03	027Fh (639d) if CGM[7:0] = "00h"
1		$\begin{array}{c c c c c c c c c c c c c c c c c c c $
2		035Fh (863d) if CGM[7:0] = "70h"
		$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$
Default	CGMI(7:0) = "50n" (480 x 800): 0 ≤ PSL[15:0], PEL[15:0] ≤ 719 (02CFh), PEL-PSL] ≤ 719 (02 CGM[7:0] = "00h" (480 x 720): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-PSL] ≤ 639 (027 CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-PSL] ≤ 639 (027 Status Availability Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Status Default Value Pst(15:0] Default Value Power On Sequence Ooth O35Fh (863d) if CGM[7:0] = "70h" O35Fh (853d) if CGM[7:0] = "00h" O31Fh (799d) if CGM[7:0] = "50h" O2Fh (39d) if CGM[7:0] = "60h" O000h Status Pst(15:0] O35Fh (853d) if CGM[7:0] = "70h" Were On Sequence O000h O31Fh (799d) if CGM[7:0] = "70h" O35Fh (853d) if CGM[7:0] = "70h" O355h (853d) if CGM[7:0] = "70h" O35Fh (853d) if CGM[7:0] = "50h" O2Fh (199d) if CGM[7:0] = "50h" O2Fh (199d) if CGM[7:0] = "6h" O35Fh (853d) if CGM[7:0] = "70h" O35Fh (853d) if CGM[7:0] = "50h" O2Fh (639d) if CGM[7:0] = "70h" O35Fh (853d) if CGM[7:0] = "70h" <t< td=""></t<>	
	S/W Reset	02CFh (719d) if CGM[7:0] = "28h"
Restriction CGM[7:0] = "70h" (480 x 864): 0 ≤ PSL[15:0], PELI15:0] ≤ 863 (035Fh), PEL-F CGM[7:0] = "6Bh" (480 x 854): 0 ≤ PSL[15:0], PEL[15:0] ≤ 853 (035Fh), PEL-F CGM[7:0] = "00h" (480 x 800): 0 ≤ PSL[15:0], PEL[15:0] ≤ 719 (02CFh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), PEL-F Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Status PSL[15:0] PELF Power On Sequence 0000h 035Fh (863d) if C 035Fh (863d) if	· /	
N -		
	Sleep In Yes Status Default Value PSL[15:0] PEL[15:0] 035Fh (863d) if CGM[7:0] 035Fh (863d) if CGM[7:0] 0000h 035Fh (853d) if CGM[7:0] 0000h 027Fh (639d) if CGM[7:0] 027Fh (639d) if CGM[7:0] 027Fh (639d) if CGM[7:0] 0000h 035Fh (863d) if CGM[7:0] 0000h 035Fh (863d) if CGM[7:0] 0000h 035Fh (863d) if CGM[7:0] 0167h (359d) if CGM[7:0] 035Fh (863d) if CGM[7:0] 035Fh (863d) if CGM[7:0] 035Fh (863d) if CGM[7:0] 0167h (359d) if CGM[7:0] 035Fh (853d) if CGM[7:0] 035Fh (863d) if CGM[7:0] 035Fh (853d) if CGM[7:0] 035Fh (853d) if CGM[7:0] 035Fh (853d) if CGM[7:0]	035Fh (863d) if CGM[7:0] = "70h"
Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Status Default Value PSL(15:0) PEL[15:0] Power On Sequence 0000h 0000h 035Fh (683d) if CGM[7:035Fh (683d) if CGM[7:035Fh (683d) if CGM[7:035Fh (683d) if CGM[7:027Fh (639d) if CGM[7:035Fh (683d) if CGM[7:035Fh (719d)	0355h (853d) if CGM[7:0] = "6Bh"	
	CGM[7:0] = "70h" (480 x 864): 0 ≤ PSL[15:0], PEL[15:0] ≤ 863 (035Fh), IPEL-PS CGM[7:0] = "6Bh" (480 x 854): 0 ≤ PSL[15:0], PEL[15:0] ≤ 853 (0355h), IPEL-PS CGM[7:0] = "50h" (480 x 800): 0 ≤ PSL[15:0], PEL[15:0] ≤ 719 (02CFh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0], PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0] PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0] PEL[15:0] ≤ 639 (027Fh), IPEL-PS CGM[7:0] = "00h" (480 x 640): 0 ≤ PSL[15:0] PEL[15:0] ≤ 639 (027Fh), IPEL-PS Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Sleep In Yes Sleep In Yes Sleep In Yes SW Reset O000h 035Fh (683d) if CG 035Fh (683d) if CG	031Fh (799d) if CGM[7:0] = "50h"
	H/W Kesei	02CFh (719d) if CGM[7:0] = "28h"
	Status Availability Register Availability Status PSL[15:0] ESL[15:0] PSL[15:0] <	· · · · ·
		· · · · · · · · · · · · · · · · · · ·

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		hbA	ress						Pa	ramet	er						
Inst / Para	R/W	MIPI		D[15:8] (Non-M	IPI)	D7	D6		D5	D4	D3	D2		D1	I	D
TEOFF	Write	34h	3400h			,	No	Argum	ent ((0000	h in MD	DI I/F)					
DTE: "-" Don't car	e		<u>a</u> <u> </u>														
Description	This c	ommano	d is used	to turn Of	FF (Act	ive Lo	w) the	e Teari	ng E	Effect	output s	signal fi	rom the	TE	E sign	al I	in
Restriction	This c	ommano	d has no (effect whe	en Tear	ring E	ffect o	utput is	s alr	eady (OFF.						
Register Availability	1	Normal N Normal N Partial N Partial N	Availability Yes Yes Yes														
				Sleep In	, -					.C		Yes					_
Default		Status Power On Sequence S/W Reset H/W Reset						Default Value Tearing Effect off Tearing Effect off Tearing Effect off									
Flow Chart		TE Line Output ON TEOFF(34h)										Legen ommai aramet	nd er				
			TE	Line Out	put Of	F	l					Action Mode equent transfe					

TEOFF: Tearing Effect Line OFF (3400h)

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TEON: Tearing Effect Line ON (3500h)

last / D-		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
TEON	Write	35h	3500h	00h	-	-	-	-	-	-	-	М
IOTE: "-" Don't car	e											
	This c	ommano	d is used	to turn ON the Tearing	ng Effec	t output	signal	from the	e TE sig	nal line.	This ou	tput is
		-	•	ng MADCTL bit ML.								
				e On has one parame	eter, whi	ch desc	ribes th	e mode	of the	Tearing	Effect C	output
			n't Care)	aring Effect Output lin	o consi	ete of V	Blankin	a inform	nation o	nlv		
	VVIICII	WI = 0			t _v		Diamini	t _{vdh}		iny.	Π	
Description		Ver Sca	tival Time ale			-				A		2
	When	M = "1"	The Tea	aring Effect Output lin	e consi	sts of bo	oth V-BI	anking a	and H-E	linking i	nformat	ion.
					t _{vo}	1		t _{vdh}	\rightarrow			
		Ver Sca	tival Time ale									
	Note:	Durina S	Sleen In I	Mode with Tearing Et	fect Lin	on T	arina F	ffect O		will be	active I	ofw
Restriction				effect when Tearing					nput pr			0/11
Hootholion	11110 0						<u>anoudy</u>		ブボ			
			n I	Status	Ŭ	_ (\gg	Av	ailability	1		
		Normal N	Mode On	, Idle Mode Off, Slee	p Out				Yes	/		
Register				, Idle Mode On, Slee			Ś		Yes			
Availability				Idle Mode Off, Sleep					Yes			
		Partial N	lode On	Idle Mode On, Sleep	o Out				Yes			
_ \\ (\ _ \) 🕅	<u> </u>			Sleep In					Yes			
		- ~ ((
		$HH \not>$				1						
		1 <i>1</i>	Š.	Status					ault Valu			
Default		<u>U</u>		On Sequence					ng Effec			
				S/W Reset					ng Effec ng Effec			
			Г					Team	ig Ellec			
]			7		
								Leç	gend			
			(TE Line Output OFF)							
								Com	mand			
								Para	meter /	7¦		
				TEON(35h)			ľ		\equiv	i -		
Flow Chart				· · · · · · · · · · · · · · · · · · ·	_				play	li –		
			/	/ TE Mode Parameter (M)	/				tion >			
			L		/		l		ode	i		
							Í					
			(TE Line Output ON)		İ		uentia			
)		i	ud				
							<u>!</u>			_ 1		

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Inst / Para	R/W	Ac	ddress					Parame	ter				
ilist / Fala		MIPI	Others	D[15:8] (Non-N	/IPI)	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	Write	36h	3600h	00h		MY	MX	MV	ML	RGB	MH	RSMX	RSM
NOTE: "-" Don't car	e											8	
	This	comma	nd defines	read/write scar	nning	directio	n of fran	ne mem	ory.				
	This	comma	nd makes	no change on th	ne oth	er drive	r status						
	В	it	Ν	AME				DES	SCRIPT	ION			
	1	ЛY	Row Addre	ess Order	Tho	co 2 hit	o o o o o tro	le interf	ano to n	omorvu	writo/ro	ad direc	tion
	1	ЛХ	Column Ad	ldress Order						ern chan			lion.
	1	٨V	Row/Colun	nn Exchange	me	benavi		spiay an		menan	geu.		
	I	VL '	Vertical Re	fresh Order			ertical re / behavi			control.			1
	R	GB	RGB-BGR	Order	"0" =	= RGB d	tor switc color sec / behavi	quence,	"1" = B	GR colo	r seque	ence	
	٢	/ []	Horizontal Order	Refresh	\sim		orizonta / behavi			on contr	ol		
	R	SMX	Flip Horizo	ntal			play im / behavi						
	R	SMY	Flip Vertica		-		splay im / behavi			Ŋ.			
Description	M				VL: V	ertical	Refresh	Order					
NON		M	Top-Le	ft (0,0) Memor	y 		Send Send Send Send	2nd 3rd	ft (0,0)		y		
			Top-Le	ft (0,0) Memor	У			Top-Le	eft (0,0)	Displa	y		
		M	L="1"				Send L Send 2 Send 2 Send 2	2nd >					

MADCTL: Memory Data Access Control (3600h)

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NT35510

IDMOFF: Idle Mode Off (3800h)

Inst / Para	R/W	Add	lress				Parame	ter				
ilist / Fara	n/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	DC
IDMOFF	Write	38h	3800h		No /	Argumei	nt (0000	h in ME	DDI I/F)			
IOTE: "-" Don't care	9											
Description	This c	ommano	d is used	to recover from Idle n	node or	l						
				play panel can displa								
Restriction	This c	ommano	d has no	effect when module is	alread	ly in Idle	Off mo	de.				
				Status				Av	ailability	y	n	
	1	Normal N	Mode On	, Idle Mode Off, Sleep	Out				Yes	a R		
Register Availability				, Idle Mode On, Sleep					Yes	<u>' \ </u>		2
Availability				Idle Mode Off, Sleep				20	Yes		Dr	
		Partial N		Idle Mode On, Sleep	Out				Yes			
				Sleep In					Yes			
				~	πÍC					3		
				Status				Dete	ault Valı	10		
			Deview				4		Mode of			
Default				On Sequence /W Reset		6	$\gg \mathbb{R}$		Mode d			
				/W Reset	(Mode d			
	20			W neser			J		woue c			
<u> </u>	<i>M</i>	// //			\mathbf{H}							
		ζη,			ラピ	3		[— — -	Legen	<u>а</u> – –		
$\mathcal{M}(\mathcal{M})$	U	-		\mathbb{A}				į	Logon	ŭ I		
		n ((Idle On Mode)			1		\neg		
	6	_ \\ (\							ommai	ndi		
U		A		\bot					aromot			
		\mathbb{N}							aramet	<u>.er</u>		
			Γ	IDMOFF(38h)					Display	<u>, j</u>		
Flow Chart									Dispia	<u></u> ¦		
				. ↓				$\langle \langle \rangle$	Action	>!		
					١					<u> </u>		
				Idle Off Mode	/				Mode	\square		
								1/s	equent	ia		
									transfe			
										I		
										'		

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IDMON: Idle Mode On (3900h)

Inst / Para	R/W	Add	lress				F	Parame	eter				
illst / Fala		MIPI	Others	D[15:8] (N	Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	DO
IDMON	Write	39h	3900h			No	Argumen	it (000	0h in MD	DI I/F)			
OTE: "-" Don't car	е												
	In the	idle on ı	node, col	to enter in or express ame Memo	sion is red	uced. T	•	-		ondary	colors u	sing MS	B of
Description				mory									
NON		Black Blue Red agenta Green Cyan Yellow	R7R6R5F 0XX 0XX 1XX 1XX 0XX 0XX 0XX	Memory (R ₄ R ₃ R ₂ R ₁ I XXXXX XXXXX XXXXX XXXXX XXXXX XXXXX XXXX		$\cdot \cdot$	G ₂ G ₁ G ₀ (XX (XX (XX) (XX) (XX) (XX) (XX) (XX)	B7B6 0 1 0 1 0 0 1 0 0	B5B4B3B XXXXXX XXXXXX XXXXXX XXXXXX XXXXXX XXXX				
Restriction	This c	ommano	d has no e	effect whe	n module	is alrea	dy in Idle	On m	ode				
Register Availability		Normal I Partial N	Vode On, Iode On, Iode On,	Status Idle Mode Idle Mode Idle Mode Idle Mode Sleep In	e On, Slee Off, Slee	ep Out p Out			Ava	ailabilit Yes Yes Yes Yes Yes	у		
Default			S	Status On Seque /W Reset /W Reset	ence				ldle Idle	ult Val Mode o Mode o Mode o	off off		





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Inst / Para	R/W	Add	lress				Parame	ter				
inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
COLMOD	Write	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF
DTE: "-" Don't care	9											
				to define the format		3 picture	data, wł	nich is to	be trai	nsferred	via the	RGB
		-	formats	are shown in the tabl	e:							
		Bit		NAME				DESCF	RIPTION			
		IPF3				0101" = 1 0110" = 1	•					
Description		IPF1 F	Pixel Forn	nat for RGB Interface	2)))) 1 1 1 " = 2	-			0	Π	
Description		IPF0				he other	•			$\Lambda \parallel$		
		PF3			"(0101" = 1	6-bit/pi	kel	M	1//		2
	IF	PF2	Divol Form	nat for Control Interfa	"(0110" = 1	8-bit/pi	cel 🔪	N N	<u>\</u> U		
	IF	PF1			"()111" = 2			<u>'</u> ()			
	IF	PF0				he other	s = not c	defined				
Restriction	There	is no vis	sible effe	ct until the Frame Me	emory i	s written	to.					
					V	l v		n	シデ			
			1	Status	l_{a}			Av	ailability			
Degister	1	Normal	Mode On	, Idle Mode Off, Slee	p Out				Yes			
Register Availability				, Idle Mode On, Slee			$\overline{\mathbf{C}}$		Yes			
1				Idle Mode Off, Sleep					Yes			
		Partial N	Node On,	, Idle Mode On, Sleep	o Out				Yes			
		V ·		Sleep In					Yes			
	·	~~ ((\mathcal{A}									
	-fi	_ 	Powe	Status				Deta	ault Valu 77h	Je		
Default				r On Sequence S/W Reset					77h			
				I/W Reset					77h			
			•									
								[— — -	- -			
			_					i	Legen			
			(2	4-bit/pixel Mode						<u></u>		
								i Co	ommai	nd		
				•					oromot	7		
				COLMOD(3Ah)					aramet			
Elow Chart								$\left \right $	Display	<u>, i</u>		
Flow Chart			<u> </u>		7			i 🖊	Display	<u></u>		
				Parameter PF[3:0] = "0110"	/			$\langle \cdot \rangle$	Action	>		
					/				Mode	<u> </u>		
			~	•					mode			
			(1	8-bit/pixel Mode					equent			
			\sim						transfe	r <u> </u> ¦		
								L		i		
				150						Vora		

COLMOD: Interface Pixel Format (3A00h)

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RAMWRC: Memory Write Continue (3C00h)

Inst / Para	R/W	Add	ress				Parame	ter				
ilist / Fala	U/ 88	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
RAMWRC	Write	3Ch	3C00h	D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
OTE: "-" Don't car	е											
Description	contin This c When Colum The S Then Sendi	ue mem ommand this cor nn/Start I tart Colu D[23:0] i ng any o	ory write I makes mmand i Row pos Imn/Start s stored ther com	t Row positions are d in frame memory and imand can stop Fram	ory Writ er driver mn reg ifferent d the co re Write	te (2Ch) r status. ister an in accor lumn reg	" comm d the rc dance v gister ar	and. ow regis vith MAI nd the re	ster are DCTL se ow regis	not res etting ter incre	et to the	e Sta
Restriction	There	is no re	striction of	on length of paramete	ers. No	access i	in the fra	ame me	mory in	Sleep I	n mode	
Register Availability Default		Normal N Partial M Partial M	Mode On fode On, fode On, Sta ower On S/W	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In Sleep In tus Sequence Reset	o Out	Con	tents of tents of	Default ¹ memory	y is set i y is set i	randomi	y	
			H/W	Reset		Con	tents of	memor	y is set i	randoml	у	
Flow Chart				RAMWRC(3Ch) Image Data 1[23:0], D2[23:0], , Dn[23:0] Any Command			1 	Corr Para Dis Ac	ameter splay ction ode uential			

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RAMRDC: Memory Read Continue (3E00h)

last / Dara	R/W	Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
RAMRDC	Read	3Eh	3E00h	D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
OTE: "-" Don't car	е		H									
Description	contin This c When Colum The S Then incren	ue mem ommand this cor nn/Start I tart Colu D[23:0] nented	ory write I makes mmand i Row pos Imn/Star is read	d to transfer data fro after "RAMRD Memo no change to the oth s accepted, the colu itions. t Row positions are d back from the fram	ory Rea er driver mn reg ifferent ne merr	d (2Eh)' r status. ister an in accor iory and	d the ro d the ro dance v d the co	and. ow regis vith MAI	ster are	not res etting.	et to the	e Sta
Restriction				on length of parameter				ame me	mory in	Sleep I	n mode	
Register Availability Default		Normal I Partial M Partial M	Mode On Tode On Tode On Sta S/W	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In tus Sequence Reset Reset	p Out	Con	tents of tents of	Default ^v memory	y is set i y is set i	randoml	y	
Flow Chart				RAMRDC(3Eh) Image Data 1[23:0], D2[23:0], , Dn[23:0] Any Command			1 	Corr Para Dis Ac	gend amand ameter splay ode uential nsfer	7		

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Inst / Para	R/W	Add	ress				Parame	ter				
ilisi / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
STESL	Write	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8
STESL	white	4411	4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0
IOTE: "-" Don't car	е											
Description	displa The T Line n Note t The T This c alread	y module earing E node. Th <u>Ver</u> Sca hat STE earing E comman ly on, th	e reache ffect Line le Tearin tival Time ale SL with I ffect Out d takes e TE out	n the display module's s line N. The TE sign e On has one parame g Effect Output line of V[15:0]="000h" is equ put line shall be activ affect on the frame tput shall continue to of until the end of the	al is not eter, whi onsists tivalent re low w followin o operation	to TEOP hen the g the c	d by cha cribes th anking in N with M display	anging I e mode nformati t _{vdh} 1="0" module rame.	MADCTI of the 7 on only.	eep in n e, if the	Effect O	output
Restriction	Para For CO Para For CO Para For CO Para For CO	meter ra GM[7:0] meter ra GM[7:0] meter ra GM[7:0] GM[7:0]	nge 0 ≦ = "6Bh" nge 0 ≦ = "50h" (nge 0 ≦ = "28h" (nge 0 ≦ = "00h" ($\begin{array}{rrrr} 480 \times 864 \mbox{ resolution} \\ N[15:0] & 864 \mbox{ (03)} \\ 480 \times 854 \mbox{ resolution} \\ N[15:0] & 854 \mbox{ (03)} \\ 480 \times 800 \mbox{ resolution} \\ N[15:0] & 800 \mbox{ (03)} \\ 480 \times 720 \mbox{ resolution} \\ N[15:0] & 720 \mbox{ (02)} \\ 480 \times 640 \mbox{ resolution} \\ N[15:0] & 640 \mbox{ (02)} \\ \end{array}$	860h)) 856h) (20h) 2D0h)		3		551			
Register Availability	1	Normal I Partial N	Mode On Iode On, Iode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out o Out			Av	vailability Yes Yes Yes Yes Yes	/		
Default			S	Status On Sequence /W Reset /W Reset					ault Valu 0000h 0000h 0000h	le		

STESL: Set Tearing Effect Scan Line (4400h~4401h)

11/8/2010





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Version 0.00



GSL: Get Scan Line (4500h~4501h)

Inst / Para	R/W	Add	ress				Parame	ter				
inst / i aia	11/99	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GSL	Read	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8
USL	neau	4511	4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0
OTE: "-" Don't car	е											
Description	scan I first lir	ines on ne of V S	display is Sync and	the current scan line s defined as VSYNC is denoted as Line 0 e, the returned value	+ VBP	+ VAD						
Restriction	-	in Sleep		e, the returned value	is unde	ineu.				6	- îl	
Register Availability		Normal I Partial N	Mode On Iode On, Iode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out			Av	ailability Yes Yes Yes Yes Yes			
Default Flow Chart				Status On Sequence W Reset W Reset GSL(45h) GSL(45h) Send Parameter N[15:8] Send Parameter N[7:0]	7		Host		ault Valu (XXXh (XXXh (XXXh Legen ommar aramet Display Action Mode equent transfe			

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last / Dava		A	ddress					Parame	eter							
Inst / Para	R/W	MIP		D[15:8] (Non-	MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
DPCKRGB	Write	Х	4A00h	00h		0	0	0	0	0	0	0	ICM			
NOTE: "-" Don't cai	re		-						-	-						
	This o	comma	nd is used	to select SRA	M data	input p	ath and	display	/ clock ir	n RGB ir	nterface					
		СМ		Data Wri	te to Sl	RAM			SRAM	Data Re	ead to D	isplay				
Description				Write Clock	SRA	M Data	ı Input P	ath	Inte	ernal Dis	play Clo	ock				
		0		PCLK		D[2:	3:0]				nd PCLI					
		1		SCL		SI	וכ		Ir	nternal C	Dscillato	r				
Restriction	-									~	n IN					
				Status					Av	ailability		V				
		Norma	l Mode Or	, Idle Mode Of	f, Sleep	o Out		كالا		Yes	1					
Register		Norma	ıl Mode Or	i, Idle Mode Or	n, Sleep	o Out				Yes						
Availability		Partia	l Mode On	, Idle Mode Off	, Sleep	Out				Yes	3					
		Partia	l Mode On	, Idle Mode On	, Sleep	Out				Yes						
				Sleep In		10		-	11	Yes						
				//	\mathcal{Y}		- (∂u						
			\geq			(4						
	0 E			Status		$\int $		$\underline{\bigcirc}$		ault Valu	le					
Default				r On Sequence	<u>}((``</u>					M = "0"						
		$\theta \pi$		S/W Reset		ノビ				M = "0"						
$\sim $	յև			I/W Reset	\mathbb{y}				IC	CM = "0"						
		- ~ (
	\int	\sum			_					I I	Leo	gend	7			
		Disc	lay Clock				/ Clock		١		;		, i			
					$\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $	Interna	l Oscilla	tor	/	į	<u></u>					
			¥.					_		ļ	Com	mand]			
		L D	PCKRGB	(14b)	r		RGB (4A	(h)			Para	meter	7¦			
		Ľ		(4AII)	L			N (1)		⁴ 			i			
Flow Chart			•		_		V		_	į	(Dis	play)			
		/ Pa	arameter I	CM = 1	/ F	Parame	ter ICM	= 0	/	ļ		tion				
	4	1		/				/			\geq					
			V				V					ode) į			
			Display Clo Internal Os		(Dis	splay Cl	lock by	PCLK)	İ	Sear	uential				
		\sim			\sim				,	į		nsfer	김			
													-1 -1			
	1									-			-			

DPCKRGB: Display Clock in RGB Interface (4A00h)

11/8/2010

Version 0.00



Inst / Para	R/W	Add	ress				Parame	ter				
inst / Faia		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DSTBON	Write	Х	4F00h	00h	0	0	0	0	0	0	0	DSTB
OTE: "-" Don't car	е											
Description	DSTB Notes 1. Bef Use 2. It ca	="1", en : ore setti er can no an not ex	ter deep ng this co ot write th xit Deep :	to enter deep standb standby mode. ommand, enter Sleep his register in Sleep-O Standby Mode while by Mode, input low pu	o In Moo Dut and setting	de (1000 Display bit DSTE	-On mo 3 from "	de. 1" to "0"	,	00h) first		
Restriction	-								141	11/	115	
Register Availability		Normal I Partial N	Vode On Iode On, Iode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out			Av	ailability Yes Yes Yes Yes Yes			
Default			S	Status On Sequence W Reset				DS DS	ault Valu TB = "0 TB = "0 TB = "0	,,		
Flow Chart		lau	((Sleep In and Display Off Mode DSTBM (4Fh) Parameter DSTB Deep Standby Mo		,		Com Para Dis Ac M	gend amand ameter splay ction ode uential nsfer			

DSTBON: Deep Standby Mode On (4F00h)

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WRPFD: Write Profile Value for Display (5000h~500Fh)

Inst / Para	R/W	Add	ress				Parame	ter				
ποι / Γαία		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010
			5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020
			5002h	00h	V037	V036	V035	V034	V033	V032	V031	V030
WRPFD	Write	50h	:	00h	:		••	••	:	:	:	:
			500Dh	00h	V147	V146	V145	V144	V143	V142	V141	V140
			500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150
			500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160
NOTE: "-" Don't car	e								1			
Description	This c	ommano	d is used	to define profile valu	es for d	isplay.		- ~ '				
Restriction	-							210		VU		
						all		2				
				Status	ar	1		Av	ailability	/		
D · · ·				, Idle Mode Off, Slee		2 \\'			Yes			
Register Availability				, Idle Mode On, Slee					Yes	2		
/ Wanability				Idle Mode Off, Slee			$ \mathbb{A} $		Yes Yes			
		Failiain		Sleep In			5		Yes			
		11			\int	()	$ rac{1}{2} $		100			
		20.		Status	アピ	1		Defa	ault Valı	Je		
Default			Power	On Sequence					FFh			
		5	S	W Reset					FFh			
10	Ц			I/W Reset					FFh			
		11 2						r — 1			_	
					1				Lege	end		
			r									
			l	WRPFD(50h)	J			¦r	Comm	hand	į	
						_		i L	Comm		_i	
			15	^t Parameter V01[7]	·01	/		- ¦/	Param	neter /	/ 	
			2^{n}	^d Parameter V02[7	:0]	/			_		İ	
Flow Chart			/	:	/			-	Disp	lay	i	
			/ 16	th Parameter V16[7	7:0]				Actio			
		l								\leq		
									Мос	de)	Ì	
									Seque	ential		
									trans			
									\sim		ןי ו	

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Version 0.00



WRDISBV: Write Display Brightness (5100h)

lpot / Dava		Add	ress				Parame	ter							
Inst / Para	R/W	MIPI	0	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
WRDISBV	Write	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV			
IOTE: "-" Don't car	е														
	This c	ommano	d is used	to adjust brightness	value.										
		•	ationship	o is that 00h value me	eans the	lowest	brightne	ess and	FFh va	lue mea	ans the l	nighes			
	bright				、 、				(= ()						
	D	BV[7:0]		Brightness (Ratio)				iess (%) %)					
Description		00h 01h		0/256 2/256					% 125%		1				
		:	-					0.70		AL D					
		FEh		. 255/256				99.60	9375%			2			
		FFh		256/256			/		0%						
							alí								
Restriction	The display supplier cannot use this command for tuning (e.g.								ng, etc.).						
												,			
				Status		U I		Av	ailability	5					
									Yes						
Register Availability	Normal Mode On, Idle Mode On, Sleep Out								Yes						
Availability	Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out							Yes							
		Partial N			o Out		$\overline{\mathcal{O}}$		Yes						
<u> </u>	A			Sleep In					Yes						
		<u> </u>													
_ \(()) \\	J 4-			Status		1		Dof	ault Valu	10					
			Power	On Sequence				Dela	00h	Je					
Default				S/W Reset			00h								
				I/W Reset					00h						
	L	<u>U</u>							0011						
				_					Legen	nd					
			_						0						
				WRDISBV(51h)				1							
				. ↓					Comma	nd					
				arameter DBV[7:0]	7			¦/F	arame	ter 7					
							j⁄								
Flow Chart									Displa	y)¦					
	Now Brightness														
			\langle	New Brightness	\rangle			_i<	Action						
				Loaded					Mode	\neg					
										\sim :					
									Sequen						
		transfer													
										1					

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Inst / Para	R/W	Add	ress				Parame	ter				
ilist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDISBV	Read	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV
OTE: "-" Don't car	e											
Description		ciple rel		brightness value. is that 00h value me	eans the	e lowest	brightne	ess and	FFh va	lue mea	ans the I	highe
Restriction	-											
Register Availability		Normal I Partial N	Mode On /Iode On, /Iode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out o Out			Av	ailability Yes Yes Yes Yes Yes			
Default		Status Default Value Power On Sequence 00h S/W Reset 00h H/W Reset 00h										
Flow Chart				RDDISBV(52h) Send Parameter DBV[7:0]	7		Host priver		egend mmand ameter isplay action Aode quentia ansfer			

RDDISBV: Read Display Brightness (5200h)

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WRCTRLD: Write CTRL Display (5300h)

Inst / Dava		Add	lress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	Write	53h	5300h	00h	0	0	BCTRL	А	DD	BL	DB	G
NOTE: "-" Don't car	е											
	This c	omman	d is used	to control ambient lig	ght, bri	ghtness a	and gam	ıma sett	ing.			
	BCTR	L: Brigh	tness Co	ontrol Block On/Off	-	-	-		-			
	The B	CTRL b	it is alwa	ys used to switch brig	ghtnes	s for disp	lay with	dimmin	g effect	(accord	ling to D	D bit)
	BC	TRL		DESCRIPTION					WM Pir			
		0	Off,			LEDPW		•	· ·	, 0	2	.,
		L		and KBV[7:0] are 00	h.	LEDPW						
		1	Dn, DN/17-01	and KPV[7:0] are act	ivo	LEDPW LEDPW						
			k On/Off	and KBV[7:0] are act	live	LEDFW	FUL= I		ouipui			()
				to control LABC bloc	~k			$\langle N \rangle$	JI 12	1 UU		
		A		DESCRIPTION		777	PWN	A duty fo	or LEDF	WM Pir	1	
			Off		nIr	By DB	/[7:0] of					,
			Dn				C block				(/	
	DD: D	D: Display Dimming Control On/Off										
		DD DESCRIPTION										
		0 Display dimming is off										
		Display dimming is on										
1				Dn/Off without Dimmi	~							
			-	om "On" to "Off", disp	olay br	ightness	is turned	d off wit	hout gra	adual di	mming,	even
		BL	JD="1") I	s selected. DESCRIPTION	<u> </u>				ON Pin			
Description				DESCRIPTION			IPOL="(active)	
	0	0	Off				NPOL="1	•		•	,	
U			\square				IPOL="(
	,		Dn			LEDON	IPOL="1	": outpu	ut low (f	or low a	ctive)	
	DB: D	isplay B	rightness	Manual/Automatic								
		ЭB				DESCRIP						
		0		ne user has to use thi	is setti	ng for ma	anual ad	justmer	it of the	brightne	ess to h	ave
		a	n effect.				<u> </u>					
				, information about th								
				te commands are va are used.	lid, bu	t there is	no effe	ct (exce	ept regis	sters ca	n be ch	angeo
	-			ual/Automatic								
		G		dai//diomatic	ſ	DESCRIP	TION					
			lanual. b	y GAMSET-comman								
				, information about th		d gamma	is inclu	ded in th	ne activo	e profile		
	The d			is adapted to the bright		-				•		ged a
	DD="1	1", e.g. E	BCTRL: 0)→1 or 1→0.	-	-						-
			-	ht sensing off-mode		•			-		-	
				" and G="0"). Setting				written	with "W	rite Disp	olay Brig	htnes
		•		d GAMSET-command				alwaya	working	0.00	if book!	aht -
			-	ht control on, light se rightness manual (DE				aiways	working	, even	II DACKII	ynt o
		o j anu (hispiay Di	nyniness manuai (De)=0)	are selec	เฮน.					

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PRELIMINARY

NT35510

Restriction	-	
	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
		10
	Status	Default Value
Default	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	OOh
Flow Chart	WRCTRLD(53h) Parameter: BCTRL, A, DD, BL, DB New Control Value Loaded	Legend Command Parameter Display Action Mode Sequential transfer

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RDCTRLD: Read CTRL Display Value (5400h)

Inst / Dara	R/W	Add	lress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCTRLD	Read	54h	5400h	00h	0	0	BCTRL	А	DD	BL	DB	G
NOTE: "-" Don't car	e											
	This c	omman	d returns	ambient light, brightr	ness co	ntrol and	d gamma	a settinę	g value.			
		•		ntrol Block On/Off								
		1	it is alwa	ys used to switch brig	ghtness	s for disp	lay with		-	•	ing to D	D bit)
	BC	TRL	~ "	DESCRIPTION					PWM Pi			
		0	Dff,	and 1/D/([7:0] are 00]	h		VPOL="(VPOL="1		•	•	-	'
			DBV[7.0] Dn.	and KBV[7:0] are 00	n.		VPOL= VPOL="(,
		1	,	and KBV[7:0] are act	tive		VPOL="1				<u> </u>	
	A: LA		k On/Off					212			0.000.00	· J/
				to control LABC bloc	ck.		~ 1					
		A		DESCRIPTION		7170	PWN	I duty fo	or LEDF	WM Pir	1	
		0 0	Off		111	By DB	/[7:0] of	comma	Ind "WF	DISBV	(5100h)	"
		1 On By LABC block										
	DD: D	D: Display Dimming Control On/Off										
		DD DESCRIPTION										
		0 Display dimming is off										
				mming is on	N	())	\sim					
				On/Off without Dimmi					المعالمة المراجع	م مار رم ا مان		
				om "On" to "Off", disp s selected.	biay bri	gniness	is turned		nout gra	adual di	nming,	even
		BL		DESCRIPTION				LED	ON Pin			
Description	1					LEDON	IPOL="(nigh acti	ve)
	0	0	Off				VPOL="		•	•	•	· ·
V			On				VPOL="(•			• ·
		<u> </u>				LEDPV	VPOL="	1": PWN	/I output	t (low lev	/el is du	ty)
		<u> </u>	rightness	Manual/Automatic								
)B				ESCRIP				had to		
			lanual, tr n effect.	e user has to use thi	is settir	ng for ma	anual ad	justmer	nt of the	brightne	ess to h	ave
				, information about th		brightne	ee ie ind	-ludad i	n tha ar	tive pro	filo	
				te commands are va								ander
				are used.	na, out		ne ene		opt rogi		1 00 011	ungot
				ual/Automatic								
	G DESCRIPTION											
		0 N	lanual, b	y GAMSET-comman	d							
				, information about th		-						
		-		is adapted to the bright	ghtnes	s registe	rs for di	splay w	hen bit	BCTRL	is chan	iged a
				\rightarrow 1 or 1 \rightarrow 0.	(4 10)							
			-	ht sensing off-mode					-		-	
		-		" and G="0"). Setting d GAMSET-comman				witten	VVILII VV	nte Disp	nay Drig	nunes
				nt control on, light se				alwavs	workind	, even	if backli	ght o
			-	rightness manual (DE				.,	8	,, =		5.0

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PRELIMINARY

NT35510

Restriction	-	
	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
	Status	Default Value
Default	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	loon
Flow Chart	RDCTRLD(54h) Send Parameter BCTRL, A, DD, BL, DB	Host Command Driver Parameter Display Action Mode Sequential transfer

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last / Dava		Add	Iress				Parame	ter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRCABC	Write	55h	5500h	00h	0	0	0	0	0	0	C1	C0	
NOTE: "-" Don't car	е												
Description	function are de C C C C C C C C	onality. ⁻ efined or 1))	There is p n a table l C0 0 1 0 1 1	Fur Off User Interface Image Still Picture Image Moving Picture Ima	erent m nction ge (UI-N (Still-Mo age (Mo	Nodes fo Node) ode) ving-Mo	de)		•	•			
Restriction	This r	egister i	s synchro	onized with V-sync by	l circuit.	uit. Availability							
Register Availability		Normal Partial N	Mode On Mode On, Mode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out o Out			Av	ailability Yes Yes Yes Yes Yes				
Default			n s	Status On Sequence W Reset				Defa	ault Valı 00h 00h 00h	he			
Flow Chart		7.2	Pit	WRCABC(55h) Parameter: C[1:0] xel Compensation and Gating Function ON/OFF	7				Leger comma carame Displa Action Mode	nd ter y / / / /ia			

WRCABC: Write Content Adaptive Brightness Control (5500h)

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Inst / Para	R/W	Add	ress				Parame	ter				
insi / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCABC	Read	56h	5600h	00h	0	0	0	0	0	0	C1	C0
DTE: "-" Don't car	е											
	functio	onality.			•	•			•	•		
Description	0		0	Off	ICTION							
	0		1	User Interface Imag	ne (111-N	(Inde)				6	Π	
	1		0	Still Picture Image		,				A IN		
			1	Moving Picture Ima		,	de)		191			
Restriction	-											
restriction	-											
				Status					ailabilit	,		1
		Jormal I	Mada On	, Idle Mode Off, Slee				AV	Yes	×		
Register				, Idle Mode On, Slee	<u> </u>				Yes	>		
Availability				Idle Mode Off, Sleep			- 1		Yes			
,				Idle Mode On, Sleep			\approx		Yes			
		r artiar i		Sleep In	/ Out			<u> </u>	Yes			
			>				S		100			
Default			S	Status On Sequence W Reset /W Reset	<u>ار</u>			Defa	ault Valı 00h 00h 00h	Je		
Flow Chart		U		RDCABC(56h)	7		Host Driver		Leger Comma Parame Displa Action Mode Eequen transfe			

RDCABC: Read Content Adaptive Brightness Control (5600h)

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WRHYSTE: Write Hysteresis (5700h~573Fh)

Inst / Para	R/W	Add	ress				Parame	ter				
IIISt / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	DC
			5700h	00h	l0115	l0114	10113	l0112	l0111	10110	1019	101
			5701h	00h	l017	l016	l015	l014	1013	l012	l011	101
			5702h	00h	10215	10214	10213	10212	10211	10210	1029	102
			5703h	00h	1027	1026	1025	1024	1023	1022	l021	102
			:	00h	ln15	ln14	In13	ln12	ln11	In10	ln9	In
			:	00h	ln7	In6	In5	In4	ln3	ln2	In1	In
			571Ch	00h	l1515	l1514	l1513	l1512	l1511	11510	1159	115
			571Dh	00h	l157	l156	l155	l154	1153	1152	V151	115
			571Eh	00h	l1615	l1614	l1613	J1612	11611	11610	l169	116
WRHYSTE	Write	57h	571Fh	00h	l167	l166	l165	l164	1163	1162	l161	116
WHITISTE	white	5711	5720h	00h	D0115	D0114	D0113	D0112	D0111	D0110	D019	D0
			5721h	00h	D017	D016	D015	D014	D013	D012	D011	D0
			5722h	00h	D0215	D0214	D0213	D0212	D0211	D0210	D029	D0
			5723h	00h	D027	D026	D025	D024	D023	D022	D021	D0
			. n: []	00h	Dn15	Dn14	Dn13	Dn12	Dn11	Dn10	Dn9	Dr
			2 WS	00h	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dr
			573Ch	💊 00h 🦳	D1515	D1514	D1513	D1512	D1511	D1510	D159	D1
			573Dh	00h	D157	D156	D155	D154	D153	D152	D151	D0
		Vn.	573Eh	00h	D1615	D1614	D1613	D1612	D1611	D1610	D169	D1
_ \(()) 🌂			573Fh	00h	D167	D166	D165	D164	D163	D162	D161	D1
OTE: "-" Don't car	e 🔥											
				to define Hysteresis								
Description	-			ent values and Dn[1	-			values.				
Description			•	arameter values after 6[15 : 0] bits are alv				=Fh)" in	ternallv	if [15[1	5 · 01 h	its a
	-	-		valid and less than "6	-			,	ternally	,	0.010	115 0
Restriction	-	-				,						
				Status				Av	ailability	/		
		Normal N	Node On	, Idle Mode Off, Slee	p Out				Yes			
Register		Normal N	Node On	, Idle Mode On, Slee	p Out				Yes			
Availability				, Idle Mode Off, Slee					Yes			
		Partial M	lode On	, Idle Mode On, Slee	o Out				Yes			
				Sleep In					Yes			
				Status				Defa	ault Valu	Je		
Default			Power	^r On Sequence					FFh			
- 0.401				S/W Reset					FFh			
			ŀ	I/W Reset					FFh			

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WRGAMMSET: Write Gamma Setting (5800h~5807h)

Inst / Para	R/W	Add	ress				Parame	ter				
ilist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			5800h	00h	G023	G022	G021	G020	G013	G012	G011	G010
			5801h	00h	G043	G042	G041	G040	G033	G032	G031	G030
			5802h	00h	G063	G062	G061	G060	G053	G052	G051	G050
WRGAMMSFT	Write	58h	5803h	00h	G083	G082	G081	G080	G073	G072	G071	G070
WHOANNOLT	VVIILE	5011	5804h	00h	G103	G102	G101	G100	G093	G092	G091	G090
			5805h	00h	G123	G122	G121	G120	G113	G112	G111	G110
			5806h	00h	G143	G142	G141	G140	G133	G132	G1 31	G130
			5807h	00h	G163	G162	G161	G160	G153	G152	G151	G150
NOTE: "-" Don't car	'e							-		\\ lr		
				to define gamma set	•			ninance	level.	U UU		
	Gamn			d on command "Gan	nma Se	t (2600h			<u>v</u>			
		Gn[3:0)]	Parameter				Select		1		
Description	├───	01h		GC0		Ga	amma C		(G=2.2)			
	├───	02h 04h		GC1 GC2				served	\mathbb{K}	2		
	├───	0411 08h	- 1	GC2 GC3		-		served				
		0011	>\ <u>\</u> {				51					
Restriction			210		n		$\overline{\bigcirc}$					
		<u> </u>										
		70,		Status	ノビ			Av	ailability	/		
$\langle \Lambda (N \rangle)$, Idle Mode Off, Slee					Yes			
Register Availability				, Idle Mode On, Slee					Yes			
Availability				Idle Mode Off, Sleep					Yes			
2		Partial	lode On,	Idle Mode On, Sleep Sleep In	o Out				Yes Yes			
		$\frac{1}{2}$		Sleep In					Yes			
				Status				Defa	ault Valı	le		
Default			Power	On Sequence		1			01h			
Delault			S	W Reset					01h			
			ŀ	I/W Reset					01h			

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RDFSVM: Read FS Value MSBs (5A00h)

Inst / Para	R/W	Add	ress				Parame	ter					
113t / 1 ala	10,00	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDFSVM	Read	5Ah	5A00h	00h	FSV15	FSV14	FSV13	FSV12	FSV11	FSV10	FSV9	FSV8	
IOTE: "-" Don't car	е												
Description	has be Anoth When to the should read v If any registe FSV[1 <i>Note:</i>	een rema using re same va be rele vill also u other co ers for N 5:8] sho Althougi	oved from nand for I ead LSBs alue whe eased. Ar update N commance ISBs and puld be 00 h FSV[15]	MSBs (FSV[15:8]) or n ambient light readin LSBs (FSV[7:0]). See MSBs command, co n LSBs/MSBs are re- nd that if e.g. LSBs a ISBs. If MSBs are re- ls are received betw I LSBs should be rele on when bit 'A' of the 5:0] is 16-bit length re- t care about the para	ng. e the con prrespor ead. After re read ad at first veen LS eased. "Write (gister, to	mmand nding M er readir and the st, the no Bs read CTRL Di he valid	"Read F SBs/LSI ng both re is no ext MSE d comm isplay (S value ra	S Value Bs shou values, MSBs r Bs read hand an 5300h)" ange is (e LSBs Ild be lo register ead cor will upd d MSB comma 0 ~ 6553	(5B00h) cked so rs for M mmand, ate LSB s read nd is "0' 35 (0000	". that the SBs and the nex s. commar	y refe I LSB t LSB d, th	
Restriction	-												
Register Availability Default		Normal I Partial N	Mode On Aode On, Aode On, Power S	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In Status On Sequence W Reset	p Out o Out		5		ailability Yes Yes Yes Yes Yes ault Valu 00h 00h				
Flow Chart				RDFSVM(5Ah)	7		Host Driver		egend ommand iramete Display Action Mode equentia				

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RDFSVL: Read FS Value LSBs (5B00h)

Inst / Para	R/W	Add	lress				Parame	ter				
1113t / 1 ala	10,00	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFSVL	Read	5Bh	5B00h	00h	FSV7	FSV6	FSV5	FSV4	FSV3	FSV2	FSV1	FSV0
NOTE: "-" Don't car	е											
Description	has be Anoth When to the should read v If any registe FSV[7 <i>Note:</i>	een rem er comn using re same v d be rele vill also other c ers for N 7:0] shou Althoug	oved from nand for I ead LSBs alue whe eased. Ar update M commance ISBs and ild be 001 h FSV[15]	LSBs (FSV[7:0]) of n ambient light readin MSBs (FSV[15:8]). S s/MSBs command, co en LSBs/MSBs are re- nd that if e.g. LSBs an ISBs. If MSBs are re- ls are received betwon LSBs should be rele- n when bit 'A' of the " 5:0] is 16-bit length re- t care about the para	ng. ee the correspore ead. After re read ad at firs veen LS eased. Write Ci gister, to	comman nding M er readir and the st, the ne BBs read TRL Dis he valid	d "Read SBs/LSI ng both re is no ext MSE d comm play (53 value ra	I FS Va Bs shou values, MSBs r Bs read hand ar 300h)" c ange is (lue MSE ild be lo register ead cor will upd d MSE comman $0 \sim 6553$	3s (5A00 cked so rs for Ms nmand, ate LSB s read d is "0". 35 (0000	Dh)". that the SBs and the nex s. commar	ey refer d LSBs t LSBs nd, the
Restriction	-											
Register Availability Default		Normal I Partial N	Mode On Aode On, Aode On, Power S	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode On, Slee Idle Mode On, Slee Sleep In Status On Sequence S/W Reset	p Out o Out		5		ailability Yes Yes Yes Yes ault Valu 00h 00h 00h			
Flow Chart				RDFSVL(5Bh) Send Parameter FSV[7:0]	7		Host Driver		egend ommano iramete Display Action Mode			

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Address Parameter Inst / Para R/W MIPI Others D[15:8] (Non-MIPI) D7 D5 D0 D6 D4 D3 D2 D1 **RDMFFSVM** Read 5Ch 5C00h 00h FFSV8 FFSV15FFSV14FFSV13FFSV12FFSV11 FFSV10 FFSV9 NOTE: "-" Don't care This command returns MSBs (FFSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the median filter. Another command for LSBs (FFSV[7:0]). See the command "Read Median Filter FS Value LSBs (5D00h)". When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs Description should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs. If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released. FFSV[15:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0". Note: Although FFSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)". Restriction Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Register Normal Mode On, Idle Mode On, Sleep Out Yes Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes **Default Value** Status Default Power On Sequence 00h S/W Reset 00h 00h H/W Reset Legend RDMFFSVM(5Ch) Host Command Driver Parameter Send Parameter FFSV[15:8] Display Flow Chart Action Mode Sequentia transfer

RDMFFSVM: Read Median Filter FS Value MSBs (5C00h)

11/8/2010

Version 0.00



Address Parameter Inst / Para R/W MIPI Others D[15:8] (Non-MIPI) D7 D5 D0 D6 D4 D3 D2 D1 RDMFFSVL Read 5Dh 5D00h 00h FFSV7 FFSV5 FFSV2 FFSV0 FFSV6 FFSV4 FFSV3 FFSV1 NOTE: "-" Don't care This command returns LSBs (FDSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the median filter. Another command for MSBs (FFSV[15:8]). See the command "Read Median Filter FS Value MSBs (5C00h)". When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs Description should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs. If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released. FFSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0". Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)". Restriction Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Register Normal Mode On, Idle Mode On, Sleep Out Yes Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes **Default Value** Status Default Power On Sequence 00h S/W Reset 00h 00h H/W Reset Legend RDMFFSVL(5Dh) Host Command Driver Parameter Send Parameter FFSV[7:0] Display Flow Chart Action Mode Sequentia transfer

RDMFFSVL: Read Median Filter FS Value LSBs (5D00h)

11/8/2010

Version 0.00



Inst / Para	R/W	Add	lress				Param	rameter							
inst / Para	FT/ V V	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
WRCABCMB	Write	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMBC			
NOTE: "-" Don't car	e														
Description	In prir	This command is used to set the minimum brightness value of the display for CABC function n principle relationship is that 00h value means the lowest brightness for CABC and FFh value mear he highest brightness for CABC.													
Restriction	-														
Register Availability		Normal I Partial N	Mode Or ⁄Iode On	Status n, Idle Mode Off, Sla n, Idle Mode On, Sla , Idle Mode Off, Sla , Idle Mode On, Sla Sleep In	eep Out			A	vailabilit Yes Yes Yes Yes Yes			2			
Default				Status r On Sequence S/W Reset	2{ 2 7		S	De	fault Val 00h 00h 00h	ue					
NO/				VRCABCMB(5Eh					Leger	and					
Flow Chart				New Display uminance Value Loaded	>				Displa Action Mode Sequer transf						

WRCABCMB: Write CABC minimum brightness (5E00h)

11/8/2010

Version 0.00



Inst / Para	R/W	Add	ress				Parame	ter				
mot / raia		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCABCMB	Read	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB
DTE: "-" Don't car	е											
Description	In prin the hig CMB[7	ciple rel ghest bri	ationship ghtness inimum b	he minimum brightne is that 00h value m for CABC. rightness forCABC s	eans th	e lowes	t brightr	ness for				
Restriction	-									5		
Register Availability	1	Normal I Partial N	Node On Iode On, Iode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out o Out			AV	ailability Yes Yes Yes Yes Yes			
Default Flow Chart				Status On Sequence /W Reset /W Reset DCABCMB(5Fh) CABCMB(5Fh)	7		Host		ault Valu 00h 00h Legen ommar aramet Display Action Mode equent transfe			

RDCABCMB: Read CABC minimum brightness (5F00h)

11/8/2010

Version 0.00



Inst / Para	R/W	Add	lress				Parameter								
inst / Para	Fi/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
WRLSCC	Write	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8			
WHESCO	vvnie	0511	6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC			
DTE: "-" Don't car	e														
Description				to send the compense ensation coefficient is											
Restriction	The d	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).													
										_	1				
				Status				Av	ailability	$A \mid N$					
		Normal I	Mode On	, Idle Mode Off, Slee	p Out		Yes								
Register		Normal I	Mode On	, Idle Mode On, Slee	p Out		Yes								
Availability		Partial N	/lode On	, Idle Mode Off, Sleep	o Out				Yes						
		Partial N	<i>l</i> ode On	1/7	Yes										
		Sleep In Yes								3					
						7	~	11	ノネ						
Default			~ 1	6	Default Value										
			Powe		8000h										
					8000h										
			L L	I/W Reset	8000h										
					<u>л\</u>	3									
								I							
		~ (Legend											
	0	_ N II)) г	WRLSCC(65h)				i		<u> </u>					
U		\mathbb{N}							Comma	and I					
	Ì		_						00111110						
		V	1 st	Parameter CC[15:	8]			-¦/ī	Parame	eter /¦					
Flow Chart			_	<u> </u>				i C	Displa	ay)¦					
			2 ⁿ	^d Parameter CC[7:0	01					\equiv :					
								_ <u> </u> <	Actio	<u>n</u> ;					
				¥				\Box	Mode	 ¦					
			/	New CC					_						
			<	Value Loaded	\geq				Sequer						
									transf	eri					
	1									_					

WRLSCC: Write Light Sensor Compensation Coefficient Value (6500h~6501h)

11/8/2010

Version 0.00



Inst / Para	R/W	Add	Address Parameter											
IIISt / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
RDLSCCM	Write	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8		
OTE: "-" Don't car	e													
Description	Light S It can Defau	This command returns MSBs of the compensation coefficient value (CC[15:8]) which is stored by "Wri Light Sensor Compensation Coefficient Value (6500h)" command. It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order. Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are "1000 00 The display supplier cannot use this command for tuning (e.g. factory tuning, etc.)												
Restriction	The di	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).												
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence 80h S/W Reset 80h H/W Reset 80h													
Default										Je				
MO,				RDLSCCM(66h)	7		Host Driver		Leger	nd ter				
Flow Chart			/		/				Display Action Mode Sequen transfe					

RDLSCCM: Read Light Sensor Compensation Coefficient Value MSBs (6600h)

11/8/2010

Version 0.00


Inst / Para	R/W	Add	ress				Parame	ter					
inst / Faia		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDLSCCL	Write	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CCC	
OTE: "-" Don't cai	re												
Description	Light S It can Defau	Sensor (read MS It value f	Compens SBs/LSBs for comp		ue (650 ⁻ mpensa s 1.0 (10	1h)" con Ition Co 000 0000	nmand. efficient 0 0000 (value" 0000 in 1	with any binary).	/ order. MSBs a	-		
Restriction	The d	display supplier cannot use this command for tuning (e.g. factory tuning, etc.).											
Register Availability		Normal I Partial N	Iormal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence 00h										
Default		Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence 00h SW Reset 00h HW Reset 00h Command Command											
	<u> </u>	M		Send Parameter	7			-		nd			
Flow Chart				CC[7:0]	/				Displa Action Mode Sequen transfe				

RDLSCCL: Read Light Sensor Compensation Coefficient Value LSBs (6700h)

11/8/2010

Version 0.00



Inst / Para	R/W	Add	lress				Parame	ter				
inst / Para	rt/ vv	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBWLB	Read	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy
OTE: "-" Don't car	е											
Description	Black:	ommano Bkx ano Wx ano	d Bky	the lowest bits of bla	ck and	white cc	lor char	acterist	ic.			
Restriction	-											
Register Availability	1	Normal I	Mode On	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Sleep	p Out			Av	ailability Yes Yes Yes			n
		Partial N		Idle Mode On, Sleep Sleep In				Yes Yes	3			
Default	L L		S	Status On Sequence /W Reset //W Reset			After M MTP Va MTP Va MTP Va	TP alue alue	ault Valu	Before 00 00 00)h)h	
Flow Chart			S	RDBWLB(70h)	7		Host Driver		ommar aramet Display Action Mode equent transfe			

RDBWLB: Read Black/White Low Bits (7000h)

11/8/2010

Version 0.00



RDBkx: Read Bkx (7100h)

	Add	lress				Parame	ter				
n/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
Read	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2
,											
This c	omman	d returns	the Bkx bit (Bkx[9:2]) of blac	k color (characte	eristic.				
-											
			Status				Av	ailability	/		
								Yes		1	
				•				Yes	<u>a I</u> A		
								Yes			2
	Partial N	Node On,		o Out			2		<u></u>		
			Sleep In			2\[Yes			
					21111	111	Ü				
			2		p		Def	ault Vali			
			Status		-	Aftor M					
		Power	On Sequence						-		
	11			a (00)h	
M			\sim								
	n						i		 		
U		_ [2				Legen	a 1		
	n ((RDBkx(71h)						<u>1</u> !		
6	≤ 111	()				Host	i Co	ommar	nd		
	$ \mathcal{A} $	<u> </u>	V]	Driver					
	<u> </u>		end Parameter	7				aramet	er /		
							$\left \right $	Display			
			/					ызріау			
							$\langle \langle \rangle$	Action	>		
							$\left \right\rangle$	Mada	<u> </u>		
							i C	wode	\square		
							¦⁄s	equent	ial		
								transfe	r!		
	e This c -	R/W MIPI Read 71h This comman - Normal Normal Partial N	MIPI Others Read 71h 7100h This command returns - Normal Mode On Normal Mode On Partial Mode On, Partial Mode On, Partial Mode On, Partial Mode On	H/W MIPI Others D[15:8] (Non-MIPI) Read 71h 7100h 00h This command returns the Bkx bit (Bkx[9:2] - - Status Normal Mode On, Idle Mode Off, Slee Normal Mode On, Idle Mode On, Slee Partial Mode On, Idle Mode Off, Slee Partial Mode On, Idle Mode On, Slee Sleep In Status Power On Sequence S/W Reset H/W Reset	H/W MIPI Others D[15:8] (Non-MIPI) D7 Read 71h 7100h 00h Bkx9 This command returns the Bkx bit (Bkx[9:2]) of blac - Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Status Status Power On Sequence S/W Reset H/W Reset RDBkx(71h) Send Parameter	H/W MIPI Others D[15:8] (Non-MIPI) D7 D6 Read 71h 7100h 00h Bkx9 Bkx8 This command returns the Bkx bit (Bkx[9:2]) of black color of the color of t	H/W MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 Read 71h 7100h 00h Bkx9 Bkx8 Bkx7 This command returns the Bkx bit (Bkx[9:2]) of black color character - -	H/W MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 Read 71h 7100h 00h Bkx9 Bkx8 Bkx7 Bkx6 This command returns the Bkx bit (Bkx[9:2]) of black color characteristic. - - - - - - - - - - - - -	HVW MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 D3 Read 71h 7100h 00h Bkx9 Bkx8 Bkx7 Bkx6 Bkx5 This command returns the Bkx bit (Bkx[9:2]) of black color characteristic. - - - Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Status After MTP Partial Mode On, Idle Mode On, Sleep Out Yes Status After MTP Power On Sequence MTP Value HWW Reset MTP Value HWW Reset MTP Value RDBkx(71h) Host RDBkx(71h) Host Send Parameter Display Action Mode	HVW MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 D3 D2 Read 71h 7100h 00h Bkx9 Bkx8 Bkx7 Bkx6 Bkx5 Bkx4 This command returns the Bkx bit (Bkx[9:2]) of black color characteristic. This command returns the Bkx bit (Bkx[9:2]) of black color characteristic.	HVW MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 D3 D2 D1 Read 71h 7100h 00h Bkx9 Bkx8 Bkx7 Bkx6 Bkx5 Bkx4 Bkx3 This command returns the Bkx bit (Bkx[9:2]) of black color characteristic. - - - Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Status After MTP Before MTP Power On Sequence MTP Value 00h HW Reset MTP Value 00h HW Reset MTP Value 00h Host RDBkx(71h) Host Send Parameter Driver Bkx[9:2] Display Action Mode

11/8/2010

Version 0.00



RDBky: Read Bky (7200h)

Inst / Para	R/W	Add	lress				Parame	ter				
ilist / Fala	U/ 1	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBky	Read	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2
OTE: "-" Don't care	9											
Description	This c	omman	d returns	the Bky bit (Bky[9:2])) of blac	k color o	characte	eristic.				
Restriction	-											
						-						
				Status				Av	ailability	/		
Register				, Idle Mode Off, Slee	•				Yes	r A	1	
Availability				, Idle Mode On, Slee	•				Yes	<u> </u>	$ + H \rightarrow $	
, wanability				Idle Mode Off, Sleep				~ {	Yes	-\\ ⊧		2
		Partial		Idle Mode On, Sleep Sleep In	Out			2	Yes Yes	. \\U	-	
						25			163			
						2						
						P \\\	V	Defa	ault Valu	le		
				Status		v	After M	TR	シデ	Before	MTP	
Default			Power	On Sequence			MTP Va	ιlue		00)h	
			3 (/ S	W Reset			MTP Va			00)h	
		25		/W Reset	<u>a</u> (MTP Va	lue		00)h	
1	<u>M</u>	<u> </u>	لار	\sim		\bigcirc						
		11,	~	angl	心	, Ú		r	 Legen	 d ¦		
	Ju	~ (\mathcal{A}	RDBky(72h)					<u> </u>	-1		
	C	\mathbb{Z}	<u> </u>				Host		ommar	nd		
U		\mathbb{N}	9	▼]	Driver					
		$\mathbb{N}_{\mathcal{I}}$		end Parameter	7			¦∠ Pa	aramete	er /		
				Bky[9:2]	/			$\frac{1}{2}$	Diaploy			
Flow Chart									Display			
								$\langle \langle \rangle$	Action	>		
									Mada	<u> </u>		
								i C	Mode	\square_{\perp}		
									equent			
									transfe	r <u> </u>		
								i				

11/8/2010

Version 0.00



RDWx: Read Wx (7300h)

Inst / Para	R/W	Add	lress				Parame	ter				
IIISt / Fala	U/ 10	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWx	Read	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx
OTE: "-" Don't car	e											
Description	This c	omman	d returns	the Wx bit (Wx[9:2])	of white	color cl	haracte	ristic.				
Restriction	-											
				Status				Av	ailability	/		
D				, Idle Mode Off, Slee					Yes		1	
Register Availability				, Idle Mode On, Slee					Yes	<u>a 10</u>		
Availability				Idle Mode Off, Sleep					Yes			2
		Partial N		Idle Mode On, Sleep	o Out			2	Yes			
				Sleep In			⇒ાર્		Yes			
						21111		U				
				2		P \\\		Defa	ault Valu			
				Status		-	After M			Before		
Default			Power	On Sequence			MTPVa					
				W Reset			MTP Va			00		
		15		W Reset	<u>a</u> (MTP Va	<u> </u>		00		
1	A			\sim			C					
				RDWx(73h)			Host Driver		Legeno	id i		
Flow Chart		U	/ s	Send Parameter Wx[9:2]	/				Display Action Mode			
									transfe			



RDWy: Read Wy (7400h)

Inst / Para	R/W	Add	ress				Parame	ter				
inst / Para	Fi/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWy	Read	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2
NOTE: "-" Don't car	е											
Description	This c	ommano	d returns	the Wy bit (Wy[9:2])	of white	color cl	haracte	ristic.				
Restriction	-											
						-						
				Status				Av	ailability	/		
Desister				, Idle Mode Off, Slee					Yes	~	1	
Register Availability				, Idle Mode On, Slee					Yes	<u> </u>		
Availability				Idle Mode Off, Sleep					Yes	<u> </u>		2
		Partial N		Idle Mode On, Sleep	Out		0	2	Yes	<u>U</u>		
				Sleep In				\Rightarrow	Yes	5		
					-	2////						
				- 0		211		Defa	ault Valu	le		
				Status		~	After M			Before	MTP	
Default			Power	On Sequence			MTP Va			00		
				W Reset			MTP Va	lue		00)h	
		25		W Reset	n		MTP Va	alue		00)h	
1	A			\sim								
NON				RDWy(74h)			Host Driver		Legeno	nd		
Flow Chart			/ s	Gend Parameter Wy[9:2]	/				Display Action Mode			
									transfe			



Inst / Para	R/W	Add	lress				Parame	ter				
inst / Para	Fi/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRGLB	Read	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy
OTE: "-" Don't car	e									-		
Description	Red: F	omman Rx and F I: Gx and	Ry	the lowest bits of red	l and gro	een colo	or chara	cteristic				
Restriction	-											
Register Availability		Normal Partial N	Mode On <i>I</i> lode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Sleep Idle Mode On, Sleep	p Out o Out		2	Av	ailability Yes Yes Yes Yes			1
		r artiar i		Sleep In					Yes	3		
Default			S	Status On Sequence /W Reset //W Reset			After M MTP Va MTP Va MTP Va	TP Ilue Ilue		Je Before 00 00 00)h)h	
Flow Chart				RDRGLB(75h)	7]	Host Driver		Legen ommar aramet Display Action Mode equent transfe			

RDRGLB: Read Red/Green Low Bits (7500h)

11/8/2010

Version 0.00



RDRx: Read Rx (7600h)

Inst / Dava	R/W	Add	lress				Parame	ter				
Inst / Para	R/VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRx	Read	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2
NOTE: "-" Don't car	е											
Description	This c	omman	d returns	the Rx bit (Rx[9:2]) o	of red co	lor char	acteristi	с.				
Restriction	-											
				Status				Av	ailability	/		
Deviater				, Idle Mode Off, Slee					Yes	~	1	
Register Availability				, Idle Mode On, Slee					Yes	<u> </u>	\underline{H}	
Availability				Idle Mode Off, Sleep					Yes	<u>+</u>		2
		Partial N	Node On,	Idle Mode On, Sleep	Out		0	2	Yes	<u></u>		
				Sleep In			ᠵᡕᡰᡰᡔ	\Rightarrow	Yes	2		
						2////						
						211	ピ	Defa	ault Valu	le		
				Status		-v	After M			Before	MTP	
Default			Power	On Sequence			MTP Va			00		
			2 N //S	W Reset			MTP Va	lue		00)h	
		25		W Reset	n (MTP Va	lue		00)h	
1	A			\sim								
NON				RDRx(76h)	كار	3			Legen	-		
		\mathbb{N}					Host		ommar			
		11/1		▼	7	[Driver		aramete	er Zi		
		V	/ s	Send Parameter	/					<u> </u>		
Flow Chart			/	Rx[9:2]					Display	·)¦		
			<u> </u>	/					A	$\overline{}$		
									Action	∕į		
								\mathbf{i}	Mode	\supset		
								- ~				
								$\left \left(\right) \right $	equent transfe			
								<u></u>		1		

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RDRy: Read Ry (7700h)

Inst / Para	R/W	Add	dress				Parame	ter				
IIISt / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRy	Read	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2
IOTE: "-" Don't car	е											
Description	This c	omman	d returns	the Ry bit (Ry[9:2]) o	f red co	lor char	acterist	ic.				
Restriction	-											
				Status				Av	ailability	/		
				, Idle Mode Off, Slee					Yes		1	
Register Availability				, Idle Mode On, Slee					Yes	<u> </u>		
Availability				, Idle Mode Off, Sleep					Yes			2
		Partial N		Idle Mode On, Sleep	o Out		_	<u> </u>	Yes	<u>_\\l</u>		
				Sleep In			સહિ		Yes			
						21111		UN N				
				0		P \\\		Defa	ault Valu	IP		
				Status			After M			Before	MTP	
Default			Power	On Sequence	 \\	-	MTPVa			00		
				W Reset			MTP Va		1), ,	00		
		25		I/W Reset	n (MTP Va	alue		00)h	
n	A			\sim								
				RDRy(77h)	J	3		— — - 	Legen	d		
	0	\mathbb{N}					Host		ommar			
U		\mathbb{N}	<u> </u>	••••••		 1	Driver			<u></u> !		
		$\mathbb{N}_{\mathcal{A}}$			7	-	511101	i <u>/</u> Pa	aramet	er /		
			/ 5	Send Parameter Ry[9:2]				1	D'	\neg		
Flow Chart									Display	<u></u>		
								$\langle \langle \rangle$	Action	>i		
										\sim		
									Mode	\square		
								1/S	equent	ia		
									transfe	rノi		



RDGx: Read Gx (7800h)

Inst / Para	R/W	Add	lress				Parame	ter				
ilist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGx	Read	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2
IOTE: "-" Don't car	e											
Description	This c	omman	d returns	the Gx bit (Gx[9:2]) c	of green	color cl	naracter	istic.				
Restriction	-											
				Status				Av	railability	/		
- • •				, Idle Mode Off, Slee					Yes		1	
Register Availability				, Idle Mode On, Slee					Yes	$A \mid A$		
Availability				Idle Mode Off, Sleep					Yes			2
		Partial N	Node On,	Idle Mode On, Sleep	o Out			2	Yes	_\\[V.	
				Sleep In			2\[Yes			
					1	2111						
				~		p		Def	ault Valu	2		
				Status			After M			Before		
Default			Power	On Sequence	121		MTP Va		2			
				S/W Reset	V		MTP Va			00		
		25		W Reset	- (MTP Va			00		
		T la				t ji			I			
NON				RDGx(78h)	<u>ار</u> 7		Host Driver		Legeno	nd		
Flow Chart				Gend Parameter Gx[9:2]	/				Display Action Mode equent			
									transfe			



RDGy: Read Gy (7900h)

Inst / Para	R/W	Add	lress				Parame	ter				
IIISt / Fala	U/ 88	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGy	Read	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2
IOTE: "-" Don't car	е											
Description	This c	omman	d returns	the Gy bit (Gy[9:2]) o	of green	color cl	naracter	istic.				
Restriction	-											
				Status				Av	ailability	/		
D				, Idle Mode Off, Slee					Yes		1	
Register Availability				, Idle Mode On, Slee					Yes			
Availability				, Idle Mode Off, Sleep					Yes			2
		Partial N	Node On,	Idle Mode On, Sleep	o Out			2	Yes	<u>\\U</u>		
				Sleep In			⇒ાર્ષ		Yes			
						2111		JU I				
				~		p		Def	ault Valu			
				Status		-	After M			Before		
Default			Power	On Sequence	191		MTPVa					
				S/W Reset			MTP Va			00		
		15		W Reset	a (MTP Va			00		
1	M			\sim			C					
		11,	The second secon	alst	<u>الر</u>			r — — - 1	Legen	d		
		- n ((\mathcal{A}	RDGy(79h)						-1İ		
	<u>C</u>	≤ 111					Host	i C	ommar	nd		
2		$ \mathcal{A} $		▼]	Driver					
		1 ~		Send Parameter	7				aramet	er /		
				Gy[9:2]				$\left \right $	Display			
Flow Chart									ызріау	¦		
								$\langle \langle \rangle$	Action	>		
									Mode	!		
								i C	NOUE	\neg		
									equent			
									transfe	ri		
								<u> </u>				



Inst / Para	R/W	Add	lress				Parame	ter				
ilist / Fala	U/ 88	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D
RDBALB	Read	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay
OTE: "-" Don't car	e											
Description	Blue:	omman Bx and I and Ay		the lowest bits of blu	e and A	color cl	haracte	ristic.				
Restriction	-											
Register Availability		Normal Partial N	Mode On ⁄Iode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	p Out o Out			Av	ailability Yes Yes Yes Yes Yes			
Default			S	Status On Sequence /W Reset /W Reset		\bigcirc	After M MTP Va MTP Va MTP Va	ITP alue alue	ault Valu	Before 00 00 00)h)h	
Flow Chart				RDBALB(7Ah)	7	[Host Driver		Legen ommar aramet Display Action Mode	nd er		

RDBALB: Read Blue/AColor Low Bits (7A00h)

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RDBx: Read Bx (7B00h)

Inst / Para	R/W	Add	lress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBx	Read	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2
OTE: "-" Don't care	9											
Description	This c	omman	d returns	the Bx bit (Bx[9:2]) o	f blue c	olor cha	racterist	tic.				
Restriction	-											
				Status				Av	ailability	/		
				, Idle Mode Off, Slee					Yes		1	
Register Availability				, Idle Mode On, Slee					Yes	<u> </u>		
Availability				Idle Mode Off, Sleep					Yes			2
		Partial N	Node On,	Idle Mode On, Sleep	o Out			2	Yes			
				Sleep In			અહિ		Yes			
						2111	111	U				
				2		p		Def	ault Valu			
				Status			After M			Before	MTP	
Default			Power	On Sequence			MTPVa					
				W Reset			MTP Va			00		
		25		W Reset	a (MTP Va			00)h	
1	M											
		711		algl	يار			r — — -	Legen	 d		
	Ju	n (($\mathcal{I}_{\mathcal{I}}$	RDBx(7Bh)					0	٦İ		
	6	<u></u>	<u>))</u>				Host	i C	ommar	id ¦		
-		$ \mathcal{A} $	<u> </u>	V]	Driver		- H- H +			
		<u> </u>		end Parameter	7				aramete	er / į		
				Bx[9:2]				$\left \right $	Display	<u> </u>		
Flow Chart									Display	¦_		
								\leq	Action	>		
									Mode			
								i C	woue	\square_{\perp}		
									equent			
									transfe	r <u> </u>		
								Ĺ		¦		

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RDBy: Read By (7C00h)

Inst / Para	R/W	Add	lress				Parame	ter				
inst / Faia		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBy	Read	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	Ву3	By2
OTE: "-" Don't car	е											
Description	This c	omman	d returns	the By bit (By[9:2]) or	f blue c	olor cha	racteris	tic.				
Restriction	-											
				Status				Av	ailability	/		
D				, Idle Mode Off, Slee					Yes		1	
Register Availability				, Idle Mode On, Slee					Yes	<u>a IR</u>		
Availability				Idle Mode Off, Sleep					Yes			2
		Partial N	Node On,	Idle Mode On, Sleep	o Out			2 f.	Yes	<u>_\\</u> [
				Sleep In			2\[Yes			
						2111		UN N				
				~		p		Def	ault Valu			
				Status		-	After M			Before		
Default			Power	On Sequence	191		MTPVa					
				W Reset			MTP Va			00		
		15		W Reset	<u>a (</u>		MTP Va			00		
1	A	11 17		\sim			C					
				RDBy(7Ch)	<u>ار</u>		Host Driver		Legen	nd		
Flow Chart			ſ	end Parameter By[9:2]	7	L	511101		aramet Display	$\leq i$		
									Action			
									Mode equent			
									transfe			



RDAx: Read Ax (7D00h)

Inst / Para	R/W	Ado	lress				Parame	ter				
inst / Para	H/VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAx	Read	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2
OTE: "-" Don't car	e											
Description	This c	omman	d returns	the Ax bit (Ax[9:2]) o	f A colo	r charac	teristic.					
Restriction	-											
				Status				Av	ailability	/		
	1	Normal	Mode On	, Idle Mode Off, Slee	p Out				Yes	~	1	
Register				, Idle Mode On, Slee					Yes			
Availability				Idle Mode Off, Sleep					Yes			2
		Partial N		Idle Mode On, Sleep	o Out			2	Yes		0-	
				Sleep In			216		Yes			
					1	2111						
				~				Dof	ault Valu			
				Status			After M		aun van	Before		
Default			Power	On Sequence			MTP Va					
				W Reset	v		MTP Va			00		
		11		W Reset	- (MTP Va			00		
4	N	11 17					C					
				alst	<u>الر</u>			 	Legen	d		
		n ((\mathcal{A}	RDAx(7Dh)						<u>1</u> !		
	<u> </u>	≤ 111	()				Host		ommar	nd		
	Ň	161.	<u> </u>	V	_]	Driver		aramet			
		U -	/ s	end Parameter	/				aramet			
Flow Chart				Ax[9:2]				$\left \right\rangle$	Display	, j		
FIOW Chart			<u> </u>					i 🖊		¦		
							$\left < \right $	Action	>			
									Mode	-, İ		
									woue			
									equent			
									transfe	ri		
								L		!		

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RDAy: Read Ay (7E00h)

Inst / Para	R/W	Add	lress				Parame	ter				
IIISt / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAy	Read	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	АуЗ	Ay2
IOTE: "-" Don't car	e											
Description	This c	omman	d returns	the Ay bit (Ay[9:2]) o	f A colo	r charac	teristic.					
Restriction	-											
				Status				Av	vailability	/		
		Normal	Mode On	, Idle Mode Off, Slee	p Out				Yes		1	
Register Availability				, Idle Mode On, Slee					Yes	<u>a 10</u>		
Availability				Idle Mode Off, Sleep					Yes			2
		Partial N		Idle Mode On, Sleep	o Out			2	Yes		6.	
				Sleep In			216		Yes			
					1	2111						
				~	11			Def	ault Valu			
				Status			After M			Before		
Default			Power	On Sequence			MTPVa		2			
				W Reset	V		MTP Va			00		
		15		/W Reset	- (MTP Va	<u> </u>	4	00		
		15 17				1			1			
	P			alst	<u>ار</u>	3		r	Legen	d		
	0)[RDAy(7Eh)			Host		ommar			
U			<u></u>	•••••••••••••••••••••••••••••••••••••••			Driver		omma			
		$\ \rho$		•	7	L		i/ P	aramet	er /¦		
			/ S	Send Parameter	/					$\exists :$		
Flow Chart				Ay[9:2]					Display	<u> </u>		
									Action	$\overline{}$		
								$ \geq$		\leq		
									Mode	_)i		
									equent			
									transfe			
								`				
								<u> </u>		1		



RDDDBS: Read DDB Start (A100h~A104h)

Inst / Para	R/W	Add	ress				Parame	ter				
llist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SIDC
			A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID
RDDDBS	Read	A1h	A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID
			A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID
			A104h	00h	1	1	1	1	1	1	1	1
NOTE: "-" Don't car	'e											
Description	comm Note: This r Contin has no interru SID[13	Note: This information is not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands are returning. Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block. This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1 st parameter has been sent => 2 nd parameter has been sent=> 0.00000000000000000000000000000000000										
Restriction	-	-	~ 1		U	6		111				
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Yes											
				Status				Defa	ault Valu	le		
							After M			Before	MTP	
Default				On Sequence		-	MTP Va			00		
				W Reset		-	MTP Va			00		
	I I		⊢	I/W Reset		1	MTP Va	du o	1	00	h	



PRELIMINARY

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RDDDBC: Read DDB Continue (A800h~A804h)

Inst / Para	R/W	Add	ress				Parame	ter				
iiist / Faia		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
RDDDBC	Read	A8h	A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MIDC
			A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
			A804h	00h	1	1	1	1	1	1	1	1
NOTE: "-" Don't car	e		-									
Description	Note: Note:	oint where RDDDBS command was interrupted by an other command. Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block. Note: For use example, 1. Set maximum return packet size=3 2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0] 3. Read 0xA8, return 2 bytes MID[15:8] and 0xFF A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue										
Restriction	comm	Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue ommand (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue ommand is undefined.										
			<u>>{}</u>	Status			$\underline{\mathbb{C}}$		ailability	,		
	24	Normal	Mode On	, Idle Mode Off, Stee	p Out		J		Yes			
Register		- 11 - 11		, Idle Mode On, Slee					Yes			
Availability				Idle Mode Off, Slee					Yes			
$\langle \langle \langle \langle \rangle \rangle \rangle \rangle$		Partial N		Idle Mode On, Slee	o Out				Yes			
		($\underline{\gamma}$	Sleep In					Yes			
		1/1.				1						
		U -		Status					ault Valu			
Default							After M			Before		
Delault				On Sequence		-	MTP Va			00		
			-	W Reset			MTP Va			00		
			F	I/W Reset			MTP Va	lue		00	h	

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RDFCS: Read First Checksum (AA00h)

Inst / Para	R/W	Add	ress				Parame	ter				
IIISt / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFCS	Read	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0
NOTE: "-" Don't car	e											
Description	registe	ers (not	include "I	the first checksum Manufacture Comma memory has been do	nd Set)							
Restriction				wait 150ms after th an read this checksu			write a	ccess c	on "Usei	r Comm	and Se	t" area
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes										
Default OOV				Status On Sequence /W Reset /W Reset RDFCS(AAh) Fend Parameter FCS[7:0]	7		Host		ault Valu 00h 00h 00h Legen ommar aramet Display Action Mode equent transfe			

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RDCCS: Read Continue Checksum (AF00h)

Inst / Para	R/W	Add	ress				Parame	ter				
IIISt / Fala	U/ 88	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCCS	Read	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0
NOTE: "-" Don't car	е											
Description	check	sum has	calculat	the continue checled from "User Commers and/or frame men	and Set	t" area r	egisters			•		
Restriction				wait 300ms after th an read this checksu					on "Use	r Comm	and Se	t" area
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesSleep InYes										
Default				Status On Sequence W Reset W Reset RDCCS(AFh) Fend Parameter CCS[7:0]	7		Host Driver		ault Vali 00h 00h 00h Legen ommar aramet Display Action Mode			

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RDID1: Read ID1 Value (DA00h)

Inst / Para	R/W	Add	lress				Parame	ter				
ilist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID1	Read	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
NOTE: "-" Don't car	re											
Description	This r	ead byte	e identifie	s the TFT LCD modu	ıle's ma	nufactur	re ID.					
Restriction	-											
				Status				Av	ailability	/		
D · · ·				, Idle Mode Off, Slee	•				Yes	ń	1	
Register Availability				, Idle Mode On, Slee					Yes	<u> </u>	-H	_
Availability				Idle Mode Off, Sleep					Yes			2
		Partial		Idle Mode On, Sleep	o Out			2	Yes	_ \}]		
	Sleep In Yes											
					1	2111		U V				
						₽₩		Defa	ault Valu	2		
				Status			After M			Before	MTP	
Default			Power	On Sequence			MTP Va			00		
				W Reset			MTP Va			00		
		215		/W Reset	n (MTP Va	alue		00)h	
1												
Flow Chart				RDID1(DAh)		Host Driver		Legen ommar aramet Display Action	nd er			
									Mode equent transfe			

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RDID2: Read ID2 Value (DB00h)

Inst / Para	R/W	Add	ress				Parame	ter				
IIISt / Fala	n/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID2	Read	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
OTE: "-" Don't care	;											
Description	made	to the d	splay, m	to track the TFT LCI aterial or construction = 80h to FFh				. It is cł	nanged	each tin	ne a vei	sion i
Restriction	-											
Register Availability	1	StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes										
Default				Status On Sequence //W Reset //W Reset //W Reset //W Reset //W Reset //W Reset //W Reset //W Reset //W Reset //W Reset	7		After M MTP Va MTP Va MTP Va		ault Vall ault Vall Legend Display Action Mode)h)h	

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RDID3: Read ID3 Value (DC00h)

Inst / Para	R/W	Add	lress				Parame	ter				
inst / Fara		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID3	Read	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
NOTE: "-" Don't car	е											
Description	This p	aramete	er read by	te identifies the TFT	LCD m	odule/dr	iver.					
Restriction	-											
				Status				Av	ailability	/		
				, Idle Mode Off, Slee					Yes	-	1	
Register Availability				, Idle Mode On, Slee	-				Yes	<u> </u>		
Availability				Idle Mode Off, Sleep				-	Yes	41		2
		Partial N		Idle Mode On, Sleep	o Out		_	2	Yes	<u>U</u>		
Sleep In								Yes	3			
					1	?\\\\						
								Dof	ault Valu	1		
				Status		<u> </u>	After M		un van	Before	MTD	
Default			Power	On Sequence	$\left\{ \mathcal{L} \right\}$		MTP Va					
				W Reset			MTP Va			00		
		21		W Reset	n		MTP Va			00		
1						\bigcirc						
	RDID3(DCh) Ho Send Parameter								ommar			
Flow Chart				ID3[7:0]					Display Action Mode equent transfe			

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7 REFERENCE APPLICATIONS

7.1 Microprocessor Interface

The display, which is using 80-series MPU interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.2 Interfacing for 80-series 16-bit MPU by Connecting IM[3:0]="0001"

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Note: Left MVDDL and MVDDA open (not used) when using 80-series MPU interface.

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The display, which is using RGB with 16-bit SPI interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.4 Interfacing for RGB with SPI by Connecting IM[3:0]="X011"

The display, which is using RGB with I2C interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.5 Interfacing for RGB with I2C by Connecting IM[3:0]="0100"

Note 1. Connecting D23, D22, D15, D14, D7 and D6 to VSSI when using 18-bit/pixel (VIPF[3:0]="0110"). Connecting D23~D21, D15, D14 and D7~ D5 to VSSI when using 16-bit/pixel (VIPF[3:0]="0101"). Note 2. Left MVDDL and MVDDA open (not used) when using RGB with SPI interface. Note 3. IM3 is used to select SCL rising or falling edge trigger for 16-bit SPI interface.

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The display, which is using MIPI DSI and the TE line, is connected to the MPU as it is illustrated below.



Fig. 7.1.6 Interfacing for MIPLOSI with TE Line by Connecting IM[3:0]="0101"

The display, which is using MIPI DSI without the TE line, is connected to the MPU as it is illustrated below.



Fig. 7.1.7 Interfacing for MIPI DSI without TE Line by Connecting IM[3:0]="0101"

Note1. Bit DSITE should be "1", the TE line is enabled, when using MIPI with TE line.

Note2. Bit DSITE should be "0", the TE line is disabled, when using MIPI without TE line. The command 35h TEON cannot active the separated TE line.

Note3. Connecting HSSI_DATA1_P/N to VSSAM when using 1 data lane application.

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The display, which is using MDDI with 16-bit SPI interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.8 Interfacing for MDDI with 16-bit SPI by Connecting IM[3:0]="X110"

The display, which is using MDDI with I2C interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.9 Interfacing for MDDI with I2CI by Connecting IM[3:0]="0111"

Notes:

1. Connecting HSSI_DATA1_P/N to VSSAM when using MDDI Type-I (1 data lane).

2. IM3 is used to select SCL rising or falling edge trigger when using 16-bit SPI interface.

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7.2 Connections with Panel



NOTES:

1. The scan direction from top to bottom indicated in above figure means (CTB XOR ML = "0"). 2. The relationship between Sn output sequence and CRL/CGM[7:0] is shown below.

CGM[7:0]	Display Resolution	Sn Output Sequence	Note
70h	480RGB x 864		
6Bh	480RGB x 854	CRL="0" S1 _(R) →S2 _(G) →S3 _(B) →…→S1438 _(R) →S1439 _(G) →S1440 _(B)	All S1 to S1440
50h	480RGB x 800	CRL="1":	are used
28h	480RGB x 720	$S1440_{(B)} \rightarrow S1439_{(G)} \rightarrow S1438_{(B)} \rightarrow \dots \rightarrow S3_{(R)} \rightarrow S2_{(G)} \rightarrow S1_{(B)}$	are used
⁹ 00h	480RGB x 640		